CHAPTER OBJECTIVES

- Become familiar with the $r_e$, hybrid, and hybrid $\pi$ models for the BJT transistor.
- Learn to use the equivalent model to find the important ac parameters for an amplifier.
- Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
- Become aware of the general ac characteristics of a variety of important BJT configurations.
- Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
- Develop some skill in troubleshooting ac amplifier networks.

5.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the ac response of the BJT amplifier by reviewing the models most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether small-signal or large-signal techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 12.

There are three models commonly used in the small-signal ac analysis of transistor networks: the $r_e$ model, the hybrid $\pi$ model, and the hybrid equivalent model. This chapter introduces all three but emphasizes the $r_e$ model.

5.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, $P_o$, of a system cannot be greater than its power
input, \( P_i \), and that the efficiency defined by \( \eta = P_o/P_i \) cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is the principal contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an “exchange” of dc power to the ac domain that permits establishing a higher output ac power. In fact, a conversion efficiency is defined by \( \eta = P_{o(ac)}/P_{i(dc)} \), where \( P_{o(ac)} \) is the ac power to the load and \( P_{i(dc)} \) is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 5.1. The resulting direction of flow is indicated in the figure with a plot of the current \( i \) versus time. Let us now insert a control mechanism such as that shown in Fig. 5.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

That is, for this example,

\[ i_{ac(p-p)} \ll i_{c(p-p)} \]

and amplification in the ac domain has been established. The peak-to-peak value of the output current far exceeds that of the control current.

For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a “clipping” (flattening) of the peak region at the high and low end of the output signal. In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other’s requirements and limitations.

However, it is extremely helpful to realize that:

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis. It happens, however, that one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions, so there is still an important link between the two types of analysis.

### 5.3 BJT Transistor Modeling

The key to transistor small-signal analysis is the use of the equivalent circuits (models) to be introduced in this chapter.

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

In the formative years of transistor network analysis the hybrid equivalent network was employed the most frequently. Specification sheets included the parameters in their listing, and analysis was simply a matter of inserting the equivalent circuit with the listed values.
The drawback to using this equivalent circuit, however, is that it is defined for a set of operating conditions that might not match the actual operating conditions. In most cases, this is not a serious flaw because the actual operating conditions are relatively close to the chosen operating conditions on the data sheets. In addition, there is always a variation in actual resistor values and given transistor beta values, so as an approximate approach it was quite reliable. Manufacturers continue to specify the hybrid parameter values for a particular operating point on their specification sheets. They really have no choice. They want to give the user some idea of the value of each important parameter so comparisons can be made between transistors, but they really do not know the user’s actual operating conditions.

In time the use of the $r_e$ model became the more desirable approach because an important parameter of the equivalent circuit was determined by the actual operating conditions rather than using a data sheet value that in some cases could be quite different. Unfortunately, however, one must still turn to the data sheets for some of the other parameters of the equivalent circuit. The $r_e$ model also failed to include a feedback term, which in some cases can be important if not simply troublesome.

The $r_e$ model is really a reduced version of the hybrid $\pi$ model used almost exclusively for high-frequency analysis. This model also includes a connection between output and input to include the feedback effect of the output voltage and the input quantities. The full hybrid model is introduced in Chapter 9.

Throughout the text the $r_e$ model is the model of choice unless the discussion centers on the description of each model or a region of examination that predetermines the model that should be used. Whenever possible, however, a comparison between models will be discussed to show how closely related they really are. It is also important that once you gain a proficiency with one model it will carry over to an investigation using a different model, so moving from one to another will not be a dramatic undertaking.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 5.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Because we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 5.4. The dc levels were simply important for determining the proper $Q$-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors $C_1$ and $C_2$ and bypass capacitor $C_3$ were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the “shorting out” of the dc biasing resistor $R_E$. Recall that capacitors assume an “open-circuit” equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.

![Transistor circuit](image)

**FIG. 5.3**
Transistor circuit under examination in this introductory discussion.
It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as $Z_i$, $Z_o$, $I_i$, and $I_o$ as defined by Fig. 5.5 be carried through properly. Even though the network appearance may change, you want to be sure the quantities you find in the reduced network are the same as defined by the original network. In both networks the input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor $R_C$.

The parameters of Fig. 5.5 can be applied to any system whether it has one or a thousand components. For all the analysis to follow in this text, the directions of the currents, the polarities of the voltages, and the direction of interest for the impedance levels are as appearing in Fig. 5.5. In other words, the input current $I_i$ and output current $I_o$ are, by definition, defined to enter the system. If, in a particular example, the output current is leaving the system rather than entering the system as shown in Fig. 5.5, a minus sign must be applied. The defined polarities for the input and output voltages are also as appearing in Fig. 5.5. If $V_o$ has the opposite polarity, the minus sign must be applied. Note that $Z_i$ is the impedance “looking into” the system, whereas $Z_o$ is the impedance “looking back into” the system from the output side. By choosing the defined directions for the currents and voltages as appearing in Fig. 5.5, both the input impedance and output impedance are defined as having positive values. For example, in Fig. 5.6 the input and output impedances for a particular system are both resistive. For the direction of $I_i$ and $I_o$, the resulting voltage across the resistive elements will have the same polarity as $V_i$ and $V_o$, respectively. If $I_o$ had been defined as the opposite direction in Fig. 5.5 a minus sign would have to be applied. For each case $Z_i = V_i/I_i$ and $Z_o = V_o/I_o$ with positive results if they all have the defined directions and polarity of Fig. 5.5. If the output current of an actual system has a direction opposite to that
of Fig. 5.5 a minus sign must be applied to the result because $V_o$ must be defined as appearing in Fig. 5.5. Keep Fig. 5.5 in mind as you analyze the BJT networks in this chapter. It is an important introduction to “System Analysis,” which is becoming so important with the expanded use of packaged IC systems.

If we establish a common ground and rearrange the elements of Fig. 5.4, $R_1$ and $R_2$ will be in parallel, and $R_C$ will appear from collector to emitter as shown in Fig. 5.7. Because the components of the transistor equivalent circuit appearing in Fig. 5.7 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin’s theorem, and so on, can be applied to determine the desired quantities.

Let us further examine Fig. 5.7 and identify the important quantities to be determined for the system. Because we know that the transistor is an amplifying device, we would expect some indication of how the output voltage $V_o$ is related to the input voltage $V_i$—the voltage gain. Note in Fig. 5.7 for this configuration that the current gain $A_i$ is defined by $A_i = I_o/I_i$.

In summary, therefore, the ac equivalent of a transistor network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

In the sections to follow, a transistor equivalent model will be introduced to complete the ac analysis of the network of Fig. 5.7.

5.4 THE $r_o$ TRANSISTOR MODEL

The $r_o$ model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage $V_i$ is equal to the voltage $V_{be}$ with the input current being the base current $I_b$ as shown in Fig. 5.8.

Recall from Chapter 3 that because the current through the forward-biased junction of the transistor is $I_E$, the characteristics for the input side appear as shown in Fig. 5.9a for various levels of $V_{BE}$. Taking the average value for the curves of Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply that of a forward-biased diode.
For the equivalent circuit, therefore, the input side is simply a single diode with a current $I_e$, as shown in Fig. 5.10. However, we must now add a component to the network that will establish the current $I_e$ of Fig. 5.10 using the output characteristics.

If we redraw the collector characteristics to have a constant $b$ as shown in Fig. 5.11 (another approximation), the entire characteristics at the output section can be replaced by a controlled source whose magnitude is beta times the base current as shown in Fig. 5.11. Because all the input and output parameters of the original configuration are now present, the equivalent network for the common-emitter configuration has been established in Fig. 5.12.

The equivalent model of Fig. 5.12 can be awkward to work with due to the direct connection between input and output networks. It can be improved by first replacing the diode by its equivalent resistance as determined by the level of $I_e$, as shown in Fig. 5.13. Recall from Section 1.8 that the diode resistance is determined by $r_D = 26 \text{ mV} / I_D$. Using the subscript $e$ because the determining current is the emitter current will result in $r_e = 26 \text{ mV} / I_E$.

Now, for the input side:

$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

Solving for $V_{be}$:

$$V_{be} = I_r e = (I_c + I_b)r_e = (\beta I_b + I_b)r_e$$

and

$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1)I_br_e}{I_b}$$

$$Z_i = (\beta + 1)r_e \equiv \beta r_e$$

(5.1)
The result is that the impedance seen “looking into” the base of the network is a resistor equal to beta times the value of $r_e$, as shown in Fig. 5.14. The collector output current is still linked to the input current by beta as shown in the same figure.

![Fig. 5.14](image)

**Fig. 5.14**

*Improved BJT equivalent circuit.*

The equivalent circuit has therefore been defined for the ideal characteristics of Fig. 5.11, but now the input and output circuits are isolated and only linked by the controlled source—a form much easier to work with when analyzing networks.

**Early Voltage**

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of beta and $I_B$, we do not have a good representation for the output impedance of the device. In reality the characteristics do not have the ideal appearance of Fig. 5.11. Rather, they have a slope as shown in Fig. 5.15 that defines the output impedance of the device. The steeper the slope, the less the output impedance and the less ideal the transistor. In general, it is desirable to have large output impedances to avoid loading down the next stage of a design. If the slope of the curves is extended until they reach the horizontal axis, it is interesting to note in Fig. 5.15 that they will all intersect at a voltage called the Early voltage. This intersection was first discovered by James M. Early in 1952. As the base current increases the slope of the line increases, resulting in an increase in output impedance with increase in base and collector current. For a particular collector and base current as shown in Fig. 5.15, the output impedance can be found using the following equation:

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CEQ}}{I_{CQ}}$$  \hspace{1cm} (5.2)

![Fig. 5.15](image)

**Fig. 5.15**

*Defining the Early voltage and the output impedance of a transistor.*
Typically, however, the Early voltage is sufficiently large compared with the applied collector-to-emitter voltage to permit the following approximation.

\[ r_o \approx \frac{V_A}{I_{CQ}} \quad (5.3) \]

Clearly, since \( V_A \) is a fixed voltage, the larger the collector current, the less the output impedance.

For situations where the Early voltage is not available the output impedance can be found from the characteristics at any base or collector current using the following equation:

\[ \text{Slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o} \]

and

\[ r_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad (5.4) \]

For the same change in voltage in Fig. 5.15 the resulting change in current \( \Delta I_C \) is significantly less for \( r_{o2} \) than \( r_{o1} \), resulting in \( r_{o2} \) being much larger than \( r_{o1} \).

In situations where the specification sheets of a transistor do not include the Early voltage or the output characteristics, the output impedance can be determined from the hybrid parameter \( h_{oe} \) that is normally plotted on every specification sheet. It is a quantity that will be described in detail in Section 5.19.

In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 5.16.

The equivalent circuit of Fig. 5.16 will be used throughout the analysis to follow for the common-emitter configuration. Typical values of beta run from 50 to 200, with values of \( \beta r_e \) typically running from a few hundred ohms to a maximum of 6 \( k\Omega \) to 7 \( k\Omega \). The output resistance \( r \) is typically in the range of 40 \( k\Omega \) to 50 \( k\Omega \).

**Common-Base Configuration**

The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. The general characteristics of the input and output circuit will generate an equivalent circuit that will approximate the actual behavior of the device. Recall for the common-emitter configuration the use of a diode to represent the connection from base to emitter. For the common-base configuration of Fig. 5.17a the \( pnp \) transistor employed will present the same possibility at the input circuit. The result is the use of a diode in the equivalent circuit as shown in Fig. 5.17b. For the output circuit, if we return to Chapter 3 and review Fig. 3.8, we find that the collector current is related to the emitter current by alpha \( \alpha \). In this case, however, the controlled source defining the collector current as inserted in Fig. 5.17b is opposite in direction to that of the controlled source of the common-emitter configuration. The direction of the collector current in the output circuit is now opposite that of the defined output current.
For the ac response, the diode can be replaced by its equivalent ac resistance determined by \( r_e = 26 \text{ mV} / I_E \) as shown in Fig. 5.18. Take note of the fact that the emitter current continues to determine the equivalent resistance. An additional output resistance can be determined from the characteristics of Fig. 5.19 in much the same manner as applied to the common-emitter configuration. The almost horizontal lines clearly reveal that the output resistance \( r_o \) as appearing in Fig. 5.18 will be quite high and certainly much higher than that for the typical common-emitter configuration.

The network of Fig. 5.18 is therefore an excellent equivalent circuit for the analysis of most common-base configurations. It is similar in many ways to that of the common-emitter configuration. In general, common-base configurations have very low input impedance because it is essentially simply \( r_e \). Typical values extend from a few ohms to perhaps 50 \( \Omega \). The output impedance \( r_o \) will typically extend into the megohm range. Because the output current is opposite to the defined \( I_o \) direction, you will find in the analysis to follow that there is no phase shift between the input and output voltages. For the common-emitter configuration there is a 180° phase shift.

![Fig. 5.17](image)

(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

![Fig. 5.18](image)

Common base \( r_e \) equivalent circuit.

![Fig. 5.19](image)

Defining \( Z_o \).
Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 5.16 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated, and the effect of using the same model will become quite apparent.

*npn versus pnp*

The dc analysis of npn and pnp configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities. However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

5.5 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The transistor models just introduced will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations will be relatively easy to examine once the content of this chapter is reviewed and understood. For each configuration, the effect of an output impedance is examined for completeness.

The computer analysis section includes a brief description of the transistor model employed in the PSpice and Multisim software packages. It demonstrates the range and depth of the available computer analysis systems and how relatively easy it is to enter a complex network and print out the desired results. The first configuration to be analyzed in detail is the common-emitter fixed-bias network of Fig. 5.20. Note that the input signal $V_i$ is applied to the base of the transistor, whereas the output $V_o$ is off the collector. In addition, recognize that the input current $I_i$ is not the base current, but the source current, and the output current $I_o$ is the collector current. The small-signal ac analysis begins by removing the dc effects of $V_{CC}$ and replacing the dc blocking capacitors $C_1$ and $C_2$ by short-circuit equivalents, resulting in the network of Fig. 5.21.

![Common-emitter fixed-bias configuration](image1)

Note in Fig. 5.21 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of $R_B$ and $R_C$ in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters $Z_i$, $Z_o$, $I_i$, and $I_o$ on the redrawn network. Substituting the $r_e$ model for the common-emitter configuration of Fig. 5.21 results in the network of Fig. 5.22.

The next step is to determine $\beta$, $r_e$, and $r_o$. The magnitude of $\beta$ is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor...
testing instrument. The value of $r_e$ must be determined from a dc analysis of the system, and the magnitude of $r_o$ is typically obtained from the specification sheet or characteristics.

Assuming that $\beta$, $r_e$, and $r_o$ have been determined will result in the following equations for the important two-port characteristics of the system.

$Z_i$  Figure 5.22 clearly shows that

$$Z_i = R_B \parallel \beta r_e \text{ ohms} \quad (5.5)$$

For the majority of situations $R_B$ is greater than $\beta r_e$ by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$Z_i \approx \beta r_e \quad R_B \approx 10 \beta r_e \quad (5.6)$$

$Z_o$  Recall that the output impedance of any system is defined as the impedance $Z_o$ determined when $V_i = 0$. For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

$$Z_o = R_C \parallel r_o \text{ ohms} \quad (5.7)$$

If $r_o \approx 10 R_C$, the approximation $R_C \parallel r_o \approx R_C$ is frequently applied, and

$$Z_o \approx R_C \quad r_o \approx 10 R_C \quad (5.8)$$

$A_v$  The resistors $r_o$ and $R_C$ are in parallel, and

$$V_o = -\beta I_b (R_C \parallel r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \parallel r_o)$$

and

$$A_v = \frac{V_o}{V_i} = \frac{(R_C \parallel r_o)}{r_e} \quad (5.9)$$

If $r_o \approx 10 R_C$, so that the effect of $r_o$ can be ignored,

$$A_v = -\frac{R_C}{r_e} \quad r_o \approx 10 R_C \quad (5.10)$$

Note the explicit absence of $\beta$ in Eqs. (5.9) and (5.10), although we recognize that $\beta$ must be utilized to determine $r_e$. \[\boxed{\text{FIG. 5.22}}\]

Substituting the $r_e$ model into the network of Fig. 5.21.

\[\boxed{\text{FIG. 5.23}}\]

Determining $Z_o$ for the network of Fig. 5.22.
Phase Relationship  The negative sign in the resulting equation for $A_v$ reveals that a $180^\circ$ phase shift occurs between the input and output signals, as shown in Fig. 5.24. This is a result of the fact that $bI_b$ establishes a current through $R_C$ that will result in a voltage across $R_C$, the opposite of that defined by $V_o$.

![Fig. 5.24](image.png)

**Demonstrating the $180^\circ$ phase shift between input and output waveforms.**

**EXAMPLE 5.1** For the network of Fig. 5.25:

a. Determine $r_e$.

b. Find $Z_i$ (with $r_o = \infty \Omega$).

c. Calculate $Z_o$ (with $r_o = \infty \Omega$).

d. Determine $A_v$ (with $r_o = \infty \Omega$).

e. Repeat parts (c) and (d) including $r_o = 50 \, \Omega$ in all calculations and compare results.

![Fig. 5.25](image.png)

**Example 5.1.**

**Solution:**

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \, \text{V} - 0.7 \, \text{V}}{470 \, \Omega} = 24.04 \, \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04 \, \mu\text{A}) = 2.428 \, \text{mA}$$

$$r_e = \frac{26 \, \text{mV}}{2.428 \, \text{mA}} = 10.71 \, \Omega$$

b. $\beta r_e = (100)(10.71 \, \Omega) = 1.071 \, k\Omega$

$$Z_i = R_B || \beta r_e = 470 \, \Omega || 1.071 \, k\Omega = 1.07 \, k\Omega$$

c. $Z_o = R_C = 3 \, k\Omega$

d. $A_v = \frac{-RC}{r_e} = \frac{-3 \, k\Omega}{10.71 \, \Omega} = -280.11$
5.6 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the voltage-divider bias network of Fig. 5.26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of $V_B$.

Substituting the $r_e$ equivalent circuit results in the network of Fig. 5.27. Note the absence of $R_E$ due to the low-impedance shorting effect of the bypass capacitor, $C_E$. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to $R_E$ that it is treated as a short circuit across $R_E$. When $V_{CC}$ is set to zero, it places one end of $R_1$ and $R_C$ at ground potential as shown in Fig. 5.27. In addition, note that $R_1$ and $R_2$ remain part of the input circuit, whereas $R_C$ is part of the output circuit. The parallel combination of $R_1$ and $R_2$ is defined by

$$R' = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

(5.11)

$Z_i$ From Fig. 5.27

$$Z_i = R' \beta r_e$$

(5.12)

$e. \ Z_o = r_o \| R_C = 50 \, k\Omega \| 3 \, k\Omega = 2.83 \, k\Omega \text{ vs. } 3 \, k\Omega$

$$A_v = \frac{-r_o \| R_C}{r_e} = \frac{2.83 \, k\Omega}{10.71 \, \Omega} = -264.24 \text{ vs. } -280.11$$

FIG. 5.26
Voltage-divider bias configuration.

FIG. 5.27
Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.26.
From Fig. 5.27 with $V_i$ set to 0 V, resulting in $I_b = 0 \mu A$ and $\beta I_b = 0 mA$,

$$Z_o = R_C \| r_o$$ \hspace{1cm} (5.13)

If $r_o \geq 10R_C$,

$$Z_o = R_C \hspace{1cm} r_o \geq 10R_C$$ \hspace{1cm} (5.14)

$A_v$ Because $R_C$ and $r_o$ are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_o}$$

so that

$$V_o = -\beta \left( \frac{V_i}{\beta r_o} \right) (R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{R_C \| r_o}{r_e}$$ \hspace{1cm} (5.15)

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e} \hspace{1cm} r_o \geq 10R_C$$ \hspace{1cm} (5.16)

Phase Relationship The negative sign of Eq. (5.15) reveals a 180° phase shift between $V_o$ and $V_i$.

EXAMPLE 5.2 For the network of Fig. 5.28, determine:

a. $r_e$.

b. $Z_i$.

c. $Z_o \left( r_o = \infty \Omega \right)$.

d. $A_v \left( r_o = \infty \Omega \right)$.

e. The parameters of parts (b) through (d) if $r_o = 50 \Omega$ and compare results.

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FIG. 5.28 Example 5.2.
Solution:

a. DC: Testing $\beta R_E > 10 R_2,$

$$R_2 \beta (90)(1.5 \, \text{k}\Omega) > 10(8.2 \, \text{k}\Omega)$$

$$135 \, \text{k}\Omega > 82 \, \text{k}\Omega \text{ (satisfied)}$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2 \, \text{k}\Omega)(22 \, \text{V})}{56 \, \text{k}\Omega + 8.2 \, \text{k}\Omega} = 2.81 \, \text{V}$$

$$V_E = V_B - V_{BE} = 2.81 \, \text{V} - 0.7 \, \text{V} = 2.11 \, \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11 \, \text{V}}{1.5 \, \text{k}\Omega} = 1.41 \, \text{mA}$$

$$r_e = \frac{26 \, \text{mV}}{1.41 \, \text{mA}} = 18.44 \, \Omega$$

b. $R' = R_1 \| R_2 = (56 \, \text{k}\Omega) \| (8.2 \, \text{k}\Omega) = 7.15 \, \text{k}\Omega$

$$Z_i = R' \| \beta r_e = 7.15 \, \text{k}\Omega \| (90)(18.44 \, \Omega) = 7.15 \, \text{k}\Omega \| 1.66 \, \text{k}\Omega$$

$$= 1.35 \, \text{k}\Omega$$

c. $Z_o = R_C = 6.8 \, \text{k}\Omega$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8 \, \text{k}\Omega}{18.44 \, \Omega} = -368.76$

e. $Z_i = 1.35 \, \text{k}\Omega$

$$Z_o = R_C \| r_o = 6.8 \, \text{k}\Omega \| 50 \, \text{k}\Omega = 5.98 \, \text{k}\Omega \text{ vs. } 6.8 \, \text{k}\Omega$$

$$A_v = -\frac{R_C}{r_e} = -\frac{5.98 \, \text{k}\Omega}{18.44 \, \Omega} = -324.3 \text{ vs. } -368.76$$

There was a measurable difference in the results for $Z_o$ and $A_v$, because the condition $r_o \geq 10 R_C$ was not satisfied.

5.7 CE Emitter-Bias Configuration

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the un bypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.29. The $r_e$ equivalent model is substituted in Fig. 5.30, but note the absence of the resistance $r_o$. The effect of $r_o$ is to make the analysis a great deal more complicated, and considering the fact that in
most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of $r_o$ will be discussed later in this section.

Applying Kirchhoff’s voltage law to the input side of Fig. 5.30 results in

$$V_i = I_b\beta r_e + I_o R_E$$

or

$$V_i = I_b\beta r_e + (\beta + 1)I_b R_E$$

and the input impedance looking into the network to the right of $R_B$ is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

The result as displayed in Fig. 5.31 reveals that the input impedance of a transistor with an unbypassed resistor $R_E$ is determined by

$$Z_b = \beta r_e + (\beta + 1)R_E$$  \hspace{1cm} (5.17)

Because $\beta$ is normally much greater than 1, the approximate equation is

$$Z_b \approx \beta r_e + \beta R_E$$  \hspace{1cm} (5.18)

Because $R_E$ is usually greater than $r_e$, Eq. (5.18) can be further reduced to

$$Z_b \approx \beta R_E$$  \hspace{1cm} (5.19)

$Z_i$  Returning to Fig. 5.30, we have

$$Z_i = R_B || Z_b$$  \hspace{1cm} (5.20)

$Z_o$  With $V_i$ set to zero, $I_b = 0$, and $\beta I_b$ can be replaced by an open-circuit equivalent. The result is

$$Z_o = R_C$$  \hspace{1cm} (5.21)

$A_v$

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta \left( \frac{V_i}{Z_b} \right) R_C$$

with

$$A_v = \frac{V_o}{V_i} = \frac{\beta R_C}{Z_b}$$  \hspace{1cm} (5.22)

Substituting $Z_b \approx \beta (r_e + R_E)$ gives

$$A_v = \frac{V_o}{V_i} \approx -\frac{R_C}{r_e + R_E}$$  \hspace{1cm} (5.23)

and for the approximation $Z_b \approx \beta R_E$,

$$A_v = \frac{V_o}{V_i} \approx -\frac{R_C}{R_E}$$  \hspace{1cm} (5.24)

Note the absence of $\beta$ from the equation for $A_v$, demonstrating an independence in variation of $\beta$.

Phase Relationship  The negative sign in Eq. (5.22) again reveals a $180^\circ$ phase shift between $V_o$ and $V_i$. 

![FIG. 5.31](image-url)
Effect of $r_o$  The equations appearing below will clearly reveal the additional complexity resulting from including $r_o$ in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through careful application of the basic laws of circuit analysis such as Kirchhoff’s voltage and current laws, source conversions, Thévenin’s theorem, and so on. The equations were included to remove the nagging question of the effect of $r_o$ on the important parameters of a transistor configuration.

$Z_i$

\[ Z_b = \beta r_e + \frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o} R_E \]  

(5.25)

Because the ratio $R_C/r_o$ is always much less than $(\beta + 1)$,

\[ Z_b \approx \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o} \]

For $r_o \geq 10(R_C + R_E)$,

\[ Z_b \approx \beta r_e + (\beta + 1)R_E \]

which compares directly with Eq. (5.17).

In other words, if $r_o \geq 10(R_C + R_E)$, all the equations derived earlier result. Because $\beta + 1 \equiv \beta$, the following equation is an excellent one for most applications:

\[ Z_b \approx \beta(r_e + R_E) \quad r_o \geq 10(R_C + R_E) \]  

(5.26)

$Z_o$

\[ Z_o = R_C\| \left[ r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right] \]  

(5.27)

However, $r_o \gg r_e$, and

\[ Z_o \approx R_C\| r_o \left[ 1 + \frac{\beta}{1 + \frac{\beta r_e}{R_E}} \right] \]

which can be written as

\[ Z_o \approx R_C\| r_o \left[ 1 + \frac{1}{\beta + \frac{r_e}{R_E}} \right] \]

Typically $1/\beta$ and $r_e/R_E$ are less than one with a sum usually less than one. The result is a multiplying factor for $r_o$ greater than one. For $\beta = 100$, $r_e = 10 \Omega$, and $R_E = 1 \text{k}\Omega$,

\[ \frac{1}{\beta + \frac{r_e}{R_E}} = \frac{1}{100 + \frac{10 \Omega}{1000 \Omega}} = \frac{1}{0.02} = 50 \]

and

\[ Z_o = R_C[51r_o] \]

which is certainly simply $R_C$. Therefore,

\[ Z_o \approx R_C \]

(5.28)

which was obtained earlier.
### BJT AC Analysis

**Av**

\[
A_v = \frac{V_o}{V_i} = \frac{-\beta R_C}{Z_b} \left[ \frac{1 + \frac{r_e}{r_o}}{1 + \frac{R_C}{r_o}} \right] + \frac{R_C}{r_o} \tag{5.29}
\]

The ratio \(\frac{r_e}{r_o} \ll 1\), and

\[
A_v \approx \frac{V_o}{V_i} \approx \frac{-\beta R_C}{Z_b} + \frac{R_C}{r_o} \left( 1 + \frac{R_C}{r_o} \right)
\]

For \(r_o \approx 10R_C\),

\[
A_v \approx \frac{V_o}{V_i} \approx -\frac{\beta R_C}{Z_b} \quad r_o \approx 10R_C
\]

as obtained earlier.

**Bypassed**

If \(R_E\) of Fig. 5.29 is bypassed by an emitter capacitor \(C_E\), the complete \(r_e\) equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.5) to (5.10) are therefore applicable.

**EXAMPLE 5.3** For the network of Fig. 5.32, without \(C_E\) (unbypassed), determine:

a. \(r_e\)

b. \(Z_i\)

c. \(Z_o\)

d. \(A_v\)

**Solution:**

a. DC:

\[
I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega + (121)0.56\ \text{k}\Omega} = 35.89\ \mu\text{A}
\]

\[
I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\ \text{mA}
\]

and \(r_e = \frac{26\ \text{mV}}{4.34\ \text{mA}} = 5.99\ \Omega\)
b. Testing the condition \( r_o \geq 10(R_C + R_E) \), we obtain
\[
40 \, \text{k}\Omega \geq 10(2.2 \, \text{k}\Omega + 0.56 \, \text{k}\Omega)
\]
\[
40 \, \text{k}\Omega \geq 10(2.76 \, \text{k}\Omega) = 27.6 \, \text{k}\Omega \text{ (satisfied)}
\]
Therefore,
\[
Z_b = \beta(r_e + R_E) = 120(5.99 \, \Omega + 560 \, \Omega) = 67.92 \, \text{k}\Omega
\]
and
\[
Z_i = R_B \| Z_b = 470 \, \text{k}\Omega \| 67.92 \, \text{k}\Omega = 59.34 \, \text{k}\Omega
\]
c. \( Z_o = R_C = 2.2 \, \text{k}\Omega \)
d. \( r_o \geq 10R_C \) is satisfied. Therefore,
\[
A_v = \frac{V_o}{V_i} \approx -\frac{\beta R_C}{Z_b} = \frac{-120(2.2 \, \text{k}\Omega)}{67.92 \, \text{k}\Omega}
\]
\[
= -3.89
\]
compared to \(-3.93\) using Eq. (5.20): \( A_v \equiv -R_C/R_E \).

**EXAMPLE 5.4** Repeat the analysis of Example 5.3 with \( C_E \) in place.

**Solution:**

a. The dc analysis is the same, and \( r_e = 5.99 \, \Omega \).
b. \( R_E \) is “shorted out” by \( C_E \) for the ac analysis. Therefore,
\[
Z_i = R_B \| Z_b = R_B \| \beta r_e = 470 \, \text{k}\Omega \| (120)(5.99 \, \Omega)
\]
\[
= 470 \, \text{k}\Omega \| 718.8 \, \Omega = 717.70 \, \Omega
\]
c. \( Z_o = R_C = 2.2 \, \text{k}\Omega \)
d. \( A_v = \frac{-R_C}{r_e} 
\]
\[
= \frac{-2.2 \, \text{k}\Omega}{5.99 \, \Omega} = -367.28 \text{ (a significant increase)}
\]

**EXAMPLE 5.5** For the network of Fig. 5.33 (with \( C_E \) unconnected), determine (using appropriate approximations):

a. \( r_e \)
b. \( Z_i \)
c. \( Z_o \)
d. \( A_v \)
**Solution:**

a. Testing $\beta R_E > 10R_2$,

$$(210)(0.68 \, k\Omega) > 10(10 \, k\Omega)$$

$142.8 \, k\Omega > 100 \, k\Omega$ (satisfied)

we have

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10 \, k\Omega}{90 \, k\Omega + 10 \, k\Omega} (16 \, V) = 1.6 \, V$$

$$V_E = V_B - V_{BE} = 1.6 \, V - 0.7 \, V = 0.9 \, V$$

$$I_E = \frac{V_E}{R_E} = \frac{0.9 \, V}{0.68 \, k\Omega} = 1.324 \, mA$$

$$r_e = \frac{26 \, mV}{1.324 \, mA} = 19.64 \, \Omega$$

b. The ac equivalent circuit is provided in Fig. 5.34. The resulting configuration is different from Fig. 5.30 only by the fact that now

$$R_B = R' = R_1 || R_2 = 9 \, k\Omega$$

---

**FIG. 5.34**

The ac equivalent circuit of Fig. 5.33.

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \approx \beta R_E = 142.8 \, k\Omega$$

$$Z_i = R_B \| Z_b = 9 \, k\Omega \| 142.8 \, k\Omega = 8.47 \, k\Omega$$

c. $Z_o = R_C = 2.2 \, k\Omega$

d. $A_v = -\frac{R_C}{R_E} = -\frac{2.2 \, k\Omega}{0.68 \, k\Omega} = -3.24$

---

**EXAMPLE 5.6** Repeat Example 5.5 with $C_E$ in place.

**Solution:**

a. The dc analysis is the same, and $r_e = 19.64 \, \Omega$.

b. $Z_b = \beta r_e = (210)(19.64 \, \Omega) \approx 4.12 \, k\Omega$

$$Z_i = R_B \| Z_b = 9 \, k\Omega \| 4.12 \, k\Omega$$

$$= 2.83 \, k\Omega$$

c. $Z_o = R_C = 2.2 \, k\Omega$

d. $A_v = -\frac{R_C}{r_e} = -\frac{2.2 \, k\Omega}{19.64 \, \Omega} = -112.02$ (a significant increase)

---

Another variation of an emitter-bias configuration is shown in Fig. 5.35. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, whereas for the ac analysis, the resistor $R_E$ in the equations above is simply $R_{E_1}$ with $R_{E_2}$ bypassed by $C_E$. 


5.8 Emitter-Follower Configuration

When the output is taken from the emitter terminal of the transistor as shown in Fig. 5.36, the network is referred to as an emitter-follower. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \approx 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal $V_i$. That is, both $V_o$ and $V_i$ attain their positive and negative peak values at the same time. The fact that $V_o$ “follows” the magnitude of $V_i$ with an in-phase relationship accounts for the terminology emitter-follower.

The most common emitter-follower configuration appears in Fig. 5.36. In fact, because the collector is grounded for ac analysis, it is actually a common-collector configuration. Other variations of Fig. 5.36 that draw the output off the emitter with $V_o \approx V_i$ will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the $r_e$ equivalent circuit into the network of Fig. 5.36 results in the network of Fig. 5.37. The effect of $r_o$ will be examined later in the section.
The input impedance is determined in the same manner as described in the preceding section:

\[ Z_i = R_B \parallel Z_b \]  \hspace{1cm} (5.31)

with

\[ Z_b = \beta r_e + (\beta + 1)R_E \]  \hspace{1cm} (5.32)

or

\[ Z_b \approx \beta (r_e + R_E) \]  \hspace{1cm} (5.33)

and

\[ Z_b \approx \beta R_E \quad R_E \gg r_e \]  \hspace{1cm} (5.34)

The output impedance is best described by first writing the equation for the current \( I_b \),

\[ I_b = \frac{V_i}{Z_b} \]

and then multiplying by \( (\beta + 1) \) to establish \( I_e \). That is,

\[ I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b} \]

Substituting for \( Z_b \) gives

\[ I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E} \]

or

\[ I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E} \]

but

\[ (\beta + 1) \approx \beta \]

and

\[ \frac{\beta r_e}{\beta + 1} \approx \frac{\beta r_e}{\beta} = r_e \]

so that

\[ I_e \approx \frac{V_i}{r_e + R_E} \]  \hspace{1cm} (5.35)

If we now construct the network defined by Eq. (5.35), the configuration of Fig. 5.38 results.

To determine \( Z_o \), \( V_i \) is set to zero and

\[ Z_o = R_E \parallel r_e \]  \hspace{1cm} (5.36)
Because $R_E$ is typically much greater than $r_e$, the following approximation is often applied:

$$Z_o \approx r_e$$  \hspace{1cm} (5.37)

**$A_v$**  
Figure 5.38 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}$$  \hspace{1cm} (5.38)

Because $R_E$ is usually much greater than $r_e$, $R_E + r_e \approx R_E$ and

$$A_v = \frac{V_o}{V_i} \approx 1$$  \hspace{1cm} (5.39)

**Phase Relationship**  
As revealed by Eq. (5.38) and earlier discussions of this section, $V_o$ and $V_i$ are in phase for the emitter-follower configuration.

**Effect of $r_o$**

$Z_i$

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}}$$  \hspace{1cm} (5.40)

If the condition $r_o \geq 10R_E$ is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$Z_b \approx \beta(r_e + R_E) \quad r_o \geq 10R_E$$  \hspace{1cm} (5.41)

$Z_o$

$$Z_o = r_o || R_E || \frac{\beta r_e}{(\beta + 1)}$$  \hspace{1cm} (5.42)

Using $\beta + 1 \approx \beta$, we obtain

$$Z_o = r_o || R_E || r_e$$

and because $r_o \gg r_e$,

$$Z_o \approx R_E || r_e \quad \text{Any } r_o$$  \hspace{1cm} (5.43)

**$A_v$**

$$A_v = \frac{(\beta + 1)R_E/Z_b}{1 + \frac{R_E}{r_o}}$$  \hspace{1cm} (5.44)

If the condition $r_o \geq 10R_E$ is satisfied and we use the approximation $\beta + 1 \approx \beta$, we find

$$A_v \approx \frac{\beta R_E}{Z_b}$$
EXAMPLE 5.7  For the emitter-follower network of Fig. 5.39, determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.
e. Repeat parts (b) through (d) with $r_o = 25 \, \text{k}\Omega$ and compare results.

**Solution:**

a. $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{12 \, \text{V} - 0.7 \, \text{V}}{220 \, \text{k}\Omega + (101)3.3 \, \text{k}\Omega} = 20.42 \, \mu\text{A}$

$b = (\beta + 1)I_B = (101)(20.42 \, \mu\text{A}) = 2.062 \, \text{mA}$

$r_e = \frac{26 \, \text{mV}}{I_E} = \frac{26 \, \text{mV}}{2.062 \, \text{mA}} = 12.61 \, \Omega$

b. $Z_b = \beta r_e + (\beta + 1)R_E$

$= (100)(12.61 \, \Omega) + (101)(3.3 \, \text{k}\Omega)$

$= 12.61 \, \Omega + 333.3 \, \text{k}\Omega$

$= 345.96 \, \text{k}\Omega \approx \beta R_E$

$Z_i = R_B \| Z_b = 220 \, \text{k}\Omega \| 334.56 \, \text{k}\Omega$

$= 132.72 \, \text{k}\Omega$

c. $Z_o = R_E \| r_e = 3.3 \, \text{k}\Omega \| 12.61 \, \Omega$

$= 12.56 \, \Omega \approx r_e$

d. $A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3 \, \text{k}\Omega}{3.3 \, \text{k}\Omega + 12.61 \, \Omega}$

$= 0.996 \approx 1$
e. Checking the condition $r_o \geq 10R_E$, we have

$$25 \, \text{k}\Omega \geq 10(3.3 \, \text{k}\Omega) = 33 \, \text{k}\Omega$$

which is not satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} = (100)(12.61 \, \Omega) + \frac{(100 + 1)(3.3 \, \Omega)}{1 + \frac{3.3 \, \text{k}\Omega}{25 \, \text{k}\Omega}}$$

$$= 1.261 \, \text{k}\Omega + 294.43 \, \text{k}\Omega$$

$$= 295.7 \, \text{k}\Omega$$

with

$$Z_j = R_b / Z_b = 220 \, \text{k}\Omega \| 295.7 \, \text{k}\Omega$$

$$= 126.15 \, \text{k}\Omega$$

vs. 132.72 kΩ obtained earlier

$$Z_o = R_E / r_o = 12.56 \, \Omega$$

as obtained earlier

$$A_v = \frac{(\beta + 1)R_E / Z_b}{1 + \frac{R_E}{r_o}} = \frac{(100 + 1)(3.3 \, \text{k}\Omega) / 295.7 \, \text{k}\Omega}{1 + \frac{3.3 \, \text{k}\Omega}{25 \, \text{k}\Omega}}$$

$$= 0.996 \approx 1$$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ is not satisfied, the results for $Z_o$ and $A_v$ are the same, with $Z_i$ only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of $r_o$ for this configuration.

The network of Fig. 5.40 is a variation of the network of Fig. 5.36, which employs a voltage-divider input section to set the bias conditions. Equations (5.31) to (5.34) are changed only by replacing $R_b$ by $R_1 / R_2$.

The network of Fig. 5.41 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor $R_C$. In this case $R_b$ is again replaced by the parallel combination of $R_1$ and $R_2$. The input impedance $Z_i$ and output impedance $Z_o$ are unaffected by $R_C$ because it is not reflected into the base or emitter equivalent networks. In fact, the only effect of $R_C$ is to determine the $Q$-point of operation.

5.9 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.42, with the common-base $r_e$ equivalent model substituted in Fig. 5.43. The transistor output impedance $r_o$ is not included for the
common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor $R_C$.

\[ Z_i = R_E || r_e \]  \hspace{1cm} (5.46)

\[ Z_o = R_C \]  \hspace{1cm} (5.47)

**$A_v$**

\[ V_o = -I_o R_C = -(I_c)R_C = \alpha I_e R_C \]

with

\[ I_e = \frac{V_i}{r_e} \]

so that

\[ V_o = \alpha \left( \frac{V_i}{r_e} \right) R_C \]

and

\[ A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \equiv \frac{R_C}{r_e} \]  \hspace{1cm} (5.48)

**$A_i$**  Assuming that $R_E \gg r_e$ yields

\[ I_e = I_i \]

and

\[ I_o = -\alpha I_e = -\alpha I_i \]

with

\[ A_i = \frac{I_o}{I_i} = -\alpha \approx -1 \]  \hspace{1cm} (5.49)

**Phase Relationship**  The fact that $A_v$ is a positive number shows that $V_o$ and $V_i$ are in phase for the common-base configuration.

**Effect of $r_o$**  For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance $R_C$ to permit the approximation $r_o || R_C \equiv R_C$.

**EXAMPLE 5.8**  For the network of Fig. 5.44, determine:

a. $r_e$

b. $Z_i$

c. $Z_o$

d. $A_v$

e. $A_i$

**FIG. 5.44**  Example 5.8.
Solution:

a. \[ I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega} = 1.3 \text{ V} = 1.3 \text{ mA} \]

\[ r_e = \frac{26 \text{ mV}}{1.3 \text{ mA}} = 20 \Omega \]

b. \[ Z_i = R_E \parallel r_e = 1 \text{ k}\Omega \parallel 20 \Omega = 19.61 \Omega \approx r_e \]

c. \[ Z_o = R_C = 5 \text{ k}\Omega \]

d. \[ A_v = \frac{R_C}{r_e} \frac{5 \text{ k}\Omega}{20 \Omega} = 250 \]

e. \[ A_i = -0.98 \equiv -1 \]

5.10 Collector Feedback Configuration

The collector feedback network of Fig. 5.45 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.46. The effects of a transistor output resistance \( r_o \) will be discussed later in the section.

\[ Z_i \]

\[ I_o = I' + \beta I_b \]

\[ I' = \frac{V_o - V_i}{R_F} \]

but

\[ V_o = -I_o R_C = -(I' + \beta I_b) R_C \]

with

\[ V_i = I_b \beta r_e \]

so that

\[ I' = -\frac{(I' + \beta I_b) R_C - I_b \beta r_e}{R_F} = -I' \frac{R_C}{R_F} - \frac{\beta I_b R_C}{R_F} - \frac{I_b \beta r_e}{R_F} \]

which when rearranged in the following:

\[ I' \left(1 + \frac{R_C}{R_F}\right) = -\beta I_b \frac{(R_C + r_e)}{R_F} \]
and finally,
\[ I' = -\beta I_b \left( R_C + r_e \right) \]

Now \[ Z_i = \frac{V_i}{I_i} \]

and
\[ I_i = I_b - I' = I_b + \beta I_b \frac{(R_C + r_e)}{R_C + R_F} \]
or
\[ I_i = I_b \left( 1 + \beta \frac{(R_C + r_e)}{R_C + R_F} \right) \]

Substituting for \( V_i \) in the above equation for \( Z_i \) leaves
\[ Z_i = \frac{V_i}{I_i} = \frac{I_b \beta r_e}{I_b \left( 1 + \beta \frac{(R_C + r_e)}{R_C + R_F} \right)} = \frac{\beta r_e}{1 + \beta \frac{(R_C + r_e)}{R_C + R_F}} \]

Since \( R_C \gg r_e \)
\[ Z_i = \frac{\beta r_e}{1 + \frac{r_e}{R_C}} \]
or
\[ Z_i = \frac{r_e}{1 + \frac{R_C}{\beta} + \frac{R_F}{R_C}} \] (5.50)

\( Z_o \) If we set \( V_i \) to zero as required to define \( Z_o \), the network will appear as shown in Fig. 5.47. The effect of \( \beta r_e \) is removed, and \( R_F \) appears in parallel with \( R_C \) and
\[ Z_o \equiv \frac{R_C}{R_F} \] (5.51)

**FIG. 5.47**
Defining \( Z_o \) for the collector feedback configuration.

\( A_v \)
\[ V_o = -I_o R_C = -(I' + \beta I_b) R_C \]
\[ = -\left( -\beta I_b \frac{(R_C + r_e)}{R_C + R_F} + \beta I_b \right) R_C \]
or
\[ V_o = -\beta I_b \left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) R_C \]

Then
\[ A_v = \frac{V_o}{V_i} = \frac{-\beta I_b \left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) R_C}{\beta r_e I_b} \]
\[ = - \left( 1 - \frac{(R_C + r_e)}{R_C + R_F} \right) \frac{R_C}{r_e} \]

For \( R_C \gg r_e \)
\[ A_v = - \left( 1 - \frac{R_C}{R_C + R_F} \right) \frac{R_C}{r_e} \]
or
\[
A_v = -\frac{(R_C^2 + R_F - R_C) R_C}{R_C + R_F} \frac{1}{r_e}
\]

and
\[
A_v = -\left(\frac{R_F}{R_C + R_F}\right) \frac{R_C}{r_e}
\]  \hspace{1cm} (5.52)

For \(R_F \gg R_C\)
\[
A_v \approx -\frac{R_C}{r_e} \quad \text{ (5.53)}
\]

**Phase Relationship** The negative sign of Eq. (5.52) indicates a 180° phase shift between \(V_o\) and \(V_i\).

**Effect of \(r_o\)**

\(Z_i\) A complete analysis without applying approximations results in
\[
Z_i = \frac{1 + \frac{R_C r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C r_o}{\beta r_e R_F} + \frac{R_C r_o}{R_F r_e}} \quad \text{ (5.54)}
\]

Applying the condition \(r_o \approx 10R_C\), we obtain
\[
Z_i \approx \frac{r_e \left[ 1 + \frac{R_C}{R_F} \right]}{\frac{1}{\beta} + \frac{1}{R_F} + \frac{R_C}{R_F r_e}} = \frac{1}{\frac{1}{r_e} + \frac{1}{\beta} + \frac{R_C}{R_F + r_e} + \frac{R_C}{R_F + R_C}}
\]

Applying \(R_C \gg r_e\) and \(\frac{R_C}{\beta}\),
\[
Z_i \approx \frac{r_e \left[ 1 + \frac{R_C}{R_F} \right]}{\frac{R_F + \beta R_C}{\beta R_F}} = \frac{1}{\frac{1}{r_e} + \frac{1}{\beta} + \frac{R_C}{R_F + R_C} + \frac{R_C}{R_F + R_C}}
\]

but, since \(R_F \gg R_C, R_F + R_C \approx R_F\) and \(\frac{R_F}{R_F + R_C} = 1\)
\[
Z_i \approx \frac{r_e}{1 + \frac{R_C}{R_F}} \quad \text{ (5.55)}
\]

as obtained earlier.

\(Z_o\) Including \(r_o\) in parallel with \(R_C\) in Fig. 5.47 results in
\[
Z_o = r_o R_C R_F \quad \text{ (5.56)}
\]

For \(r_o \approx 10R_C\),
\[
Z_o \approx R_C R_F \quad \text{ (5.57)}
\]

as obtained earlier. For the common condition of \(R_F \gg R_C\),
\[
Z_o \approx R_C \quad \text{ (5.58)}
\]
\[ A_v = -\frac{R_F}{R_C + R_F} \frac{r_e}{r_o} \]  
\hspace{1cm} (5.59)

For \( r_o \approx 10R_C \),

\[ A_v \approx -\frac{R_F}{R_C + R_F} \frac{r_e}{r_o} \]  
\hspace{1cm} (5.60)

and for \( R_F \gg R_C \)

\[ A_v \approx -\frac{R_C}{r_e} \]  
\hspace{1cm} (5.61)

as obtained earlier.

**EXAMPLE 5.9** For the network of Fig. 5.48, determine:

a. \( r_e \)

b. \( Z_i \)

c. \( Z_o \)

d. \( A_v \)

e. Repeat parts (b) through (d) with \( r_o = 20 \, \text{k}\Omega \) and compare results.

\[ \beta = 200, \, r_o = \infty \, \Omega \]

\[ \text{FIG. 5.48} \]

**Solution:**

a. \[ I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9 \, \text{V} - 0.7 \, \text{V}}{180 \, \text{k}\Omega + (200)2.7 \, \text{k}\Omega} = 11.53 \, \mu\text{A} \]

\[ I_E = (\beta + 1)I_B = (201)(11.53 \, \mu\text{A}) = 2.32 \, \text{mA} \]

\[ r_e = \frac{26 \, \text{mV}}{I_E} = \frac{26 \, \text{mV}}{2.32 \, \text{mA}} = 11.21 \, \Omega \]

b. \[ Z_i = \frac{r_e}{\beta + \frac{R_C}{R_C + R_F}} = \frac{11.21 \, \Omega}{\frac{1}{200} + \frac{2.7 \, \text{k}\Omega}{182.7 \, \text{k}\Omega}} = \frac{11.21 \, \Omega}{0.005 + 0.0148} = \frac{11.21 \, \Omega}{0.0198} = 566.16 \, \Omega \]

c. \[ Z_o = R_C + R_F = 2.7 \, \text{k}\Omega + 180 \, \text{k}\Omega = 2.66 \, \text{k}\Omega \]

d. \[ A_v = -\frac{R_C}{r_e} = -\frac{2.7 \, \text{k}\Omega}{11.21 \, \Omega} = -240.86 \]
e. \( Z_i \): The condition \( r_o \approx 10R_C \) is not satisfied. Therefore,

\[
Z_i = \frac{1 + \frac{R_C \| r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C \| r_o}{\beta r_e R_F} + \frac{R_C \| r_o}{R_F R_e}} = \frac{1 + \frac{2.7 \, \text{k}\Omega \| 20 \, \text{k}\Omega}{180 \, \text{k}\Omega}}{1 + \frac{2.38 \, \text{k}\Omega}{180 \, \text{k}\Omega}}
\]

\[
= \frac{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 5.91 \times 10^{-6} + 1.18 \times 10^{-3}}{1.64 \times 10^{-3}} = 1 + 0.013
\]

\[
= 617.7 \, \Omega \text{ vs. } 566.16 \, \Omega \text{ above}
\]

\( Z_o \):

\[
Z_o = r_o \| R_C \| R_F = 20 \, \text{k}\Omega \| 2.7 \, \text{k}\Omega \| 180 \, \text{k}\Omega
\]

\[
= 2.35 \, \text{k}\Omega \text{ vs. } 2.66 \, \text{k}\Omega \text{ above}
\]

\( A_v \):

\[
A_v = -\left( \frac{R_F}{R_C \| r_o + R_F} \right) \frac{R_C \| r_o}{r_e} = -\left[ \frac{180 \, \text{k}\Omega}{2.38 \, \text{k}\Omega \| 180 \, \text{k}\Omega} \right] \frac{2.38 \, \text{k}\Omega}{11.21}
\]

\[
= -\left[ 0.987 \right] 212.3
\]

\[
= -209.54
\]

For the configuration of Fig. 5.49, Eqs. (5.61) through (5.63) determine the variables of interest. The derivations are left as an exercise at the end of the chapter.
5.11 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 5.50 has a dc feedback resistor for increased stability, yet the capacitor \( C_3 \) will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of \( R_F \) shifted to the input or output side will be determined by the desired ac input and output resistance levels.

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 5.51.

\[
Z_i = R_F || \beta r_e \quad (5.65)
\]

\[
Z_o = R_C || R_F || r_o \quad (5.66)
\]

For \( r_o \approx 10R_C \),

\[
Z_o \approx R_C || R_F \quad r_o \approx 10R_C \quad (5.67)
\]

\[
A_v = \frac{R'}{r_o} \quad (5.68)
\]

and

\[
V_o = -\beta I_b R'
\]

but

\[
I_b = \frac{V_i}{\beta r_e}
\]
and

\[ V_o = -\beta V_i R' \]

so that

\[ A_v = \frac{V_o}{V_i} = -\frac{r_o R_F}{r_e R_C} \]

(5.68)

For \( r_o \geq 10R_C \),

\[ A_v = \frac{V_o}{V_i} \approx -\frac{R_F}{r_e} \quad r_o \geq 10R_C \]  

(5.69)

**Phase Relationship**  The negative sign in Eq. (5.68) clearly reveals a 180° phase shift between input and output voltages.

**EXAMPLE 5.10**  For the network of Fig. 5.52, determine:

a. \( r_e \)

b. \( Z_i \)

c. \( Z_o \)

d. \( A_v \)

e. \( V_o \) if \( V_i = 2 \text{ mV} \)

**Solution:**

a. DC: \( I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} \)

\[ I_E = (\beta + 1)I_B = (141)(18.6 \mu A) = 2.62 \text{ mA} \]

\[ r_e = \frac{26 \text{ mV}}{2.62 \text{ mA}} = 9.92 \Omega \]

b. \( \beta r_e = (140)(9.92 \Omega) = 1.39 \text{ k}\Omega \)

The ac equivalent network appears in Fig. 5.53.

\[ Z_i = R_F\parallel \beta r_e = 120 \text{ k}\Omega \parallel 1.39 \text{ k}\Omega \quad \approx 1.37 \text{ k}\Omega \]
c. Testing the condition \( r_o \geq 10R_C \), we find
\[
30 \text{ k\Omega} \geq 10(3 \text{ k\Omega}) = 30 \text{ k\Omega}
\]
which is satisfied through the equals sign in the condition. Therefore,
\[
Z_o = R_C \parallel R_F = 3 \text{ k\Omega} \parallel 68 \text{ k\Omega} = 2.87 \text{ k\Omega}
\]
d. \( r_o \geq 10R_C \); therefore,
\[
A_v = -\frac{R_F \parallel R_C}{r_e} = -\frac{68 \text{ k\Omega} \parallel 3 \text{ k\Omega}}{9.92 \text{ \Omega}} = -289.3
\]
e. \( |A_v| = 289.3 = \frac{V_o}{V_i} \)
\[
V_o = 289.3V_i = 289.3(2 \text{ mV}) = 0.579 \text{ V}
\]

## 5.12 EFFECT OF \( R_L \) AND \( R_S \)

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load to the output terminal and the effect of using a source with an internal resistance will be investigated. The network of Fig. 5.54a is typical of those investigated in the previous section. Because a resistive load was not attached to the output terminal, the gain is commonly referred to as the no-load gain and given the following notation:

\[
A_{vNL} = \frac{V_o}{V_i} \quad (5.70)
\]

In Fig. 5.54b a load has been added in the form of a resistor \( R_L \), which will change the overall gain of the system. This loaded gain is typically given the following notation:

\[
A_{vL} = \frac{V_o}{V_i} \quad \text{with } R_L \quad (5.71)
\]

In Fig. 5.54c both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation:

\[
A_{vs} = \frac{V_o}{V_s} \quad \text{with } R_L \text{ and } R_s \quad (5.72)
\]

The analysis to follow will show that:

*The loaded voltage gain of an amplifier is always less than the no-load gain.*
In other words, the addition of a load resistor $R_L$ to the configuration of Fig. 5.54a will always have the effect of reducing the gain below the no-load level.

Furthermore:

*The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.*

In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is:

For the same configuration $A_{vNL} > A_{vL} > A_{vs}$.

It will also be interesting to verify that:

*For a particular design, the larger the level of $R_L$, the greater is the level of ac gain.*

In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.

In addition:

*For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.*

In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain because the effect of $R_s$ will essentially be eliminated.

*For any network, such as those shown in Fig. 5.54 that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.*

The conclusions listed above are all quite important in the amplifier design process. When one purchases a packaged amplifier, the listed gain and all the other parameters are for the *unloaded situation*. The gain that results due to the application of a load or source resistance can have a dramatic effect on all the amplifier parameters, as will be demonstrated in the examples to follow.

In general, there are two directions one can take to analyze networks with an applied load and/or source resistance. One approach is to simply insert the equivalent circuit, as was demonstrated in Section 5.11, and use methods of analysis to determine the quantities of interest. The second is to define a two-port equivalent model and use the parameters determined for the no-load situation. The analysis to follow in this section will use the first approach, leaving the second method for Section 5.14.

For the fixed-bias transistor amplifier of Fig. 5.54c, substituting the $r_e$ equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig. 5.55.
It is particularly interesting that Fig. 5.55 is exactly the same in appearance as Fig. 5.22 except that now there is a load resistance in parallel with $R_C$ and a source resistance has been introduced in series with a source $V_s$.

The parallel combination of $R'_L = r_o R_C R_L \equiv R_C R_L$ and gives

$$V_o = -\beta I_b \left( R_C R_L \right)$$

so that

$$A_{vL} = \frac{V_o}{V_i} = -\frac{R_C R_L}{r_e} \quad (5.73)$$

The only difference in the gain equation using $V_i$ as the input voltage is the fact that $R_C$ of Eq. (5.10) has been replaced by the parallel combination of $R_C$ and $R_L$. This makes good sense because the output voltage of Fig. 5.55 is now across the parallel combination of the two resistors.

The input impedance is

$$Z_i = R_B \beta r_e \quad (5.74)$$

as before, and the output impedance is

$$Z_o = R_C r_o \quad (5.75)$$

as before.

If the overall gain from signal source $V_s$ to output voltage $V_o$ is desired, it is only necessary to apply the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

or

$$A_{vS} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \frac{V_i}{V_s} = A_{vL} \frac{Z_i}{Z_i + R_s}$$

so that

$$A_{vS} = \frac{Z_i}{Z_i + R_s} A_{vL} \quad (5.76)$$

Because the factor $Z_i/(Z_i + R_s)$ must always be less than one, Eq. (5.76) clearly supports the fact that the signal gain $A_{vS}$ is always less than the loaded gain $A_{vL}$.
EXAMPLE 5.11 Using the parameter values for the fixed-bias configuration of Example 5.1 with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values:

a. \( A_{vL} \)

b. \( A_{vS} \)

c. \( Z_i \)

d. \( Z_o \)

**Solution:**

a. Eq. (5.73): \( A_{vL} = \frac{R_C \left| R_L \right|}{r_e} = \frac{3 \text{ kΩ} \cdot 4.7 \text{ kΩ}}{10.71 \Omega} = \frac{-1.831 \text{ kΩ}}{10.71 \Omega} = -170.98 \) 

which is significantly less than the no-load gain of \(-280.11\).

b. Eq. (5.76): \( A_{vS} = \frac{Z_i}{Z_i + R_s} A_{vL} \)

With \( Z_i = 1.07 \text{ kΩ} \) from Example 5.1, we have 

\[
A_{vS} = \frac{1.07 \text{ kΩ}}{1.07 \text{ kΩ} + 0.3 \text{ kΩ}} (-170.98) = -133.54
\]

which again is significantly less than \( A_{vNL} \) or \( A_{vL} \).

c. \( Z_i = 1.07 \text{ kΩ} \) as obtained for the no-load situation.

d. \( Z_o = R_C = 3 \text{ kΩ} \) as obtained for the no-load situation.

The example clearly demonstrates that \( A_{vNL} > A_{vL} > A_{vS} \).

For the voltage-divider configuration of Fig. 5.56 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.57.
First note the strong similarities with Fig. 5.55, with the only difference being the parallel connection of $R_1$ and $R_2$ instead of just $R_B$. Everything else is exactly the same. The following equations result for the important parameters of the configuration:

$$A_{vl} = \frac{V_o}{V_i} = -\frac{R_C}{R_L r_e}$$  \hspace{1cm} (5.77)$$

$$Z_i = R_1 \parallel R_2 \beta r_e$$  \hspace{1cm} (5.78)$$

$$Z_o = R_C \parallel r_o$$  \hspace{1cm} (5.79)$$

For the emitter-follower configuration of Fig. 5.58 the small-signal ac equivalent network is as shown in Fig. 5.59. The only difference between Fig. 5.59 and the unloaded configuration of Fig. 5.37 is the parallel combination of $R_E$ and $R_L$ and the addition of the source resistor $R_s$. The equations for the quantities of interest can therefore be determined by simply replacing $R_E$ by $R_E \parallel R_L$ wherever $R_E$ appears. If $R_E$ does not appear in an equation, the load resistor $R_L$ does not affect that parameter. That is,

$$A_{vl} = \frac{V_o}{V_i} = \frac{R_E \parallel R_L}{R_E \parallel R_L + r_e}$$  \hspace{1cm} (5.80)$$

**FIG. 5.58**

Emitter-follower configuration with $R_s$ and $R_L$.

**FIG. 5.59**

Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.58.
DETERMINING THE CURRENT GAIN

You may have noticed in the previous sections that the current gain was not determined for each configuration. Earlier editions of this text did have the details of finding that gain, but in reality the voltage gain is usually the gain of most importance. The absence of the derivations should not cause concern because:

For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 5.60.

The current gain is defined by

\[ A_i = \frac{I_o}{I_i} \]  

(5.84)

Applying Ohm’s law to the input and output circuits results in

\[ I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L} \]

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration.

Substituting into Eq. (5.84) then results in

\[ A_{il} = \frac{I_o}{I_i} = \frac{V_o}{R_L} \cdot \frac{Z_i}{V_i} \]

and the following important equation:

\[ A_{il} = -A_{iv} \frac{Z_i}{R_L} \]  

(5.85)

The value of \( R_L \) is defined by the location of \( V_o \) and \( I_o \).
To demonstrate the validity of Eq. (5.82), consider the voltage-divider bias configuration of Fig. 5.28.

Using the results of Example 5.2, we find

\[ I_i = \frac{V_i}{Z_i} = \frac{V_i}{1.35 \, \text{kΩ}} \quad \text{and} \quad I_o = \frac{V_o}{R_L} = -\frac{V_o}{6.8 \, \text{kΩ}} \]

so that

\[ A_{iL} = \frac{I_o}{I_i} = \left( \frac{-\frac{V_o}{6.8 \, \text{kΩ}}}{\frac{V_i}{1.35 \, \text{kΩ}}} \right) = \left( \frac{V_o}{V_i} \right) \left( \frac{1.35 \, \text{kΩ}}{6.8 \, \text{kΩ}} \right) \]

\[ = -(-368.76) \left( \frac{1.35 \, \text{kΩ}}{6.8 \, \text{kΩ}} \right) = 73.2 \]

Using Eq. 5.82: \[ A_{iL} = -A_{vL} \frac{Z_i}{R_L} = -(-368.76) \left( \frac{1.35 \, \text{kΩ}}{6.8 \, \text{kΩ}} \right) = 73.2 \]

which has the same format as the resulting equation above and the same result.

The solution to the current gain in terms of the network parameters will be more complicated for some configurations if a solution is desired in terms of the network parameters. However, if a numerical solution is all that is desired, it is simply a matter of substituting the value of the three parameters from an analysis of the voltage gain.

As a second example, consider the common-base bias configuration of Section 5.9. In this case the voltage gain is

\[ A_{vL} \approx \frac{R_C}{r_e} \]

and the input impedance is

\[ Z_i \approx \frac{R_E}{r_e} \approx r_e \]

with \( R_L \) defined as \( R_C \) due to the location of \( I_o \).

The result is the following:

\[ A_{iL} = -A_{vL} \frac{Z_i}{R_L} = \left( -\frac{R_C}{r_e} \right) \left( \frac{v_e}{v_i} \right) \approx -1 \]

which agrees with the solution of that section because \( I_c \approx I_e \). Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

### 5.14 SUMMARY TABLES

The last few sections have included a number of derivations for unloaded and loaded BJT configurations. The material is so extensive that it seemed appropriate to review most of the conclusions for the various configurations in summary tables for quick comparisons. Although the equations using the hybrid parameters have not been discussed in detail at this point, they are included to make the tables complete. The use of hybrid parameters will be considered in a later section of this chapter. In each case the waveforms included demonstrate the phase relationship between input and output voltages. They also reveal the relative magnitude of the voltages at the input and output terminals.

Table 5.1 is for the unloaded situation, whereas Table 5.2 includes the effect of \( R_s \) and \( R_L \).

### 5.15 TWO-PORT SYSTEMS APPROACH

In the design process, it is often necessary to work with the terminal characteristics of a device rather than the individual components of the system. In other words, the designer is handed a packaged product with a list of data regarding its characteristics but has no access to the internal construction. This section will relate the important parameters determined for a number of configurations in the previous sections to the important parameters of this packaged system. The result will be an understanding of how each parameter of the
<table>
<thead>
<tr>
<th>Configuration</th>
<th>$Z_i$</th>
<th>$Z_o$</th>
<th>$A_v$</th>
<th>$A_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fixed-bias:</strong></td>
<td>Medium (1 kΩ)</td>
<td>Medium (2 kΩ)</td>
<td>High (−200)</td>
<td>High (100)</td>
</tr>
<tr>
<td><img src="image1.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation1.png" alt="Equation" /></td>
<td><img src="equation2.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation3.png" alt="Equation" /></td>
<td><img src="equation4.png" alt="Equation" /></td>
</tr>
<tr>
<td><strong>Voltage-divider bias:</strong></td>
<td>Medium (1 kΩ)</td>
<td>Medium (2 kΩ)</td>
<td>High (−200)</td>
<td>High (50)</td>
</tr>
<tr>
<td><img src="image2.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation5.png" alt="Equation" /></td>
<td><img src="equation6.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation7.png" alt="Equation" /></td>
<td><img src="equation8.png" alt="Equation" /></td>
</tr>
<tr>
<td><strong>Unbypassed emitter bias:</strong></td>
<td>High (100 kΩ)</td>
<td>Medium (2 kΩ)</td>
<td>Low (−5)</td>
<td>High (50)</td>
</tr>
<tr>
<td><img src="image3.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation9.png" alt="Equation" /></td>
<td><img src="equation10.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation11.png" alt="Equation" /></td>
<td><img src="equation12.png" alt="Equation" /></td>
</tr>
<tr>
<td><strong>Emitter-follower:</strong></td>
<td>High (100 kΩ)</td>
<td>Low (20 ºΩ)</td>
<td>Low (≡ 1)</td>
<td>High (−50)</td>
</tr>
<tr>
<td><img src="image4.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation13.png" alt="Equation" /></td>
<td><img src="equation14.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation15.png" alt="Equation" /></td>
<td><img src="equation16.png" alt="Equation" /></td>
</tr>
<tr>
<td><strong>Common-base:</strong></td>
<td>Low (20 ºΩ)</td>
<td>Medium (2 kΩ)</td>
<td>High (200)</td>
<td>Low (−1)</td>
</tr>
<tr>
<td><img src="image5.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation17.png" alt="Equation" /></td>
<td><img src="equation18.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation19.png" alt="Equation" /></td>
<td><img src="equation20.png" alt="Equation" /></td>
</tr>
<tr>
<td><strong>Collector feedback:</strong></td>
<td>Medium (1 kΩ)</td>
<td>Medium (2 kΩ)</td>
<td>High (−200)</td>
<td>High (50)</td>
</tr>
<tr>
<td><img src="image6.png" alt="Diagram" /></td>
<td></td>
<td></td>
<td><img src="equation21.png" alt="Equation" /></td>
<td><img src="equation22.png" alt="Equation" /></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><img src="equation23.png" alt="Equation" /></td>
<td><img src="equation24.png" alt="Equation" /></td>
</tr>
</tbody>
</table>
TABLE 5.2
BJT Transistor Amplifiers Including the Effect of $R_s$ and $R_L$

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$A_{vL} = V_o / V_i$</th>
<th>$Z_i$</th>
<th>$Z_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$-\frac{(R_L \parallel R_C)}{r_e}$</td>
<td>$R_B \beta r_e$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$-\frac{(R_L</td>
<td>R_C</td>
<td>r_o)}{r_e}$</td>
</tr>
<tr>
<td></td>
<td>$-\frac{(R_L</td>
<td>R_C)}{r_e}$</td>
<td>$R_1</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$-\frac{(R_L</td>
<td>R_C</td>
<td>r_o)}{r_e}$</td>
</tr>
<tr>
<td></td>
<td>$R_L = R_L</td>
<td>R_E$</td>
<td>$R_1</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$\equiv 1$</td>
<td>$R_1</td>
<td>R_2</td>
</tr>
<tr>
<td></td>
<td>$\equiv -\frac{(R_L</td>
<td>R_C)}{r_e}$</td>
<td>$R_E</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$\equiv -\frac{(R_L</td>
<td>R_C</td>
<td>r_o)}{r_e}$</td>
</tr>
<tr>
<td></td>
<td>$-\frac{(R_L</td>
<td>R_C)}{R_E}$</td>
<td>$R_1</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$\equiv R_C$</td>
<td>$R_1</td>
<td>R_2</td>
</tr>
</tbody>
</table>

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TABLE 5.2 (Continued)
BJT Transistor Amplifiers Including the Effect of $R_s$ and $R_L$

<table>
<thead>
<tr>
<th>Configuration</th>
<th>$A_{vL} = V_o/V_i$</th>
<th>$Z_i$</th>
<th>$Z_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$-(R_L \parallel R_C) R_E$</td>
<td>$R_B \beta (r_e + R_E)$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$-(R_L \parallel R_C) R_E$</td>
<td>$R_B \beta (r_e + R_E)$</td>
<td>$\equiv R_C$</td>
</tr>
<tr>
<td></td>
<td>$-(R_L \parallel R_C) r_e$</td>
<td>$\beta r_e R_F$</td>
<td>$R_C$</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$-(R_L \parallel R_C) r_o$</td>
<td>$\beta r_e R_F$</td>
<td>$R_C R_F r_o$</td>
</tr>
<tr>
<td></td>
<td>$-(R_L \parallel R_C) R_E$</td>
<td>$\beta R_E R_F$</td>
<td>$\equiv R_C R_F$</td>
</tr>
<tr>
<td>Including $r_o$:</td>
<td>$-(R_L \parallel R_C) R_E$</td>
<td>$\beta R_E R_F$</td>
<td>$\equiv R_C R_F$</td>
</tr>
</tbody>
</table>

packaged system relates to the actual amplifier or network. The system of Fig. 5.61 is called a two-port system because there are two sets of terminals—one at the input and the other at the output. At this point it is particularly important to realize that

_the data surrounding a packaged system is the no-load data._

This should be fairly obvious because the load has not been applied, nor does it come with the load attached to the package.

**FIG. 5.61**
_two-port system._
For the two-port system of Fig. 5.61 the polarity of the voltages and the direction of the currents are as defined. If the currents have a different direction or the voltages have a different polarity from that appearing in Fig. 5.61, a negative sign must be applied. Note again the use of the label $A_{\text{vNL}}$ to indicate that the provided voltage gain will be the no-load value.

For amplifiers the parameters of importance have been sketched within the boundaries of the two-port system as shown in Fig. 5.62. The input and output resistance of a packaged amplifier are normally provided along with the no-load gain. They can then be inserted as shown in Fig. 5.62 to represent the seated package.

For the no-load situation the output voltage is

$$V_o = A_{\text{vNL}} V_i$$  \hspace{1cm} (5.86)

due to the fact that $I = 0A$, resulting in $I_o R_o = 0V$.

The output resistance is defined by $V_i = 0V$. Under such conditions the quantity $A_{\text{vNL}} V_i$ is zero volts also and can be replaced by a short-circuit equivalent. The result is

$$Z_o = R_o$$  \hspace{1cm} (5.87)

Finally, the input impedance $Z_i$ simply relates the applied voltage to the resulting input current and

$$Z_i = R_i$$  \hspace{1cm} (5.88)

For the no-load situation, the current gain is undefined because the load current is zero. There is, however, a no-load voltage gain equal to $A_{\text{vNL}}$.

The effect of applying a load to a two-port system will result in the configuration of Fig. 5.63. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance. In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once $A_{\text{vNL}}$, $R_i$, and $R_o$ are defined for a particular configuration, the equations about to be derived can be employed.
Applying the voltage-divider rule to the output circuit results in

\[ V_o = \frac{R_L A_{NL} V_i}{R_L + R_o} \]

and

\[ A_{VL} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{NL} \]  

(5.89)

Because the ratio \( R_L / (R_L + R_o) \) is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level.

The current gain is then determined by

\[ A_{iL} = \frac{I_o}{I_i} = -\frac{V_o / R_L}{V_i / Z_i} = -\frac{V_o}{V_i} \frac{Z_i}{R_L} \]

and

\[ A_{iL} = -A_{iL} \frac{Z_i}{R_L} \]  

(5.90)

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters \( Z_i \) and \( R_L \). The next example will demonstrate the usefulness and validity of Eqs. (5.89) and (5.90).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 5.64, a source with an internal resistance has been applied to the basic two-port system. The definitions of \( Z_i \) and \( A_{NL} \) are such that:

The parameters \( Z_i \) and \( A_{NL} \) of a two-port system are unaffected by the internal resistance of the applied source.

The output impedance may be affected by the magnitude of \( R_s \).

The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 5.64 is determined by the voltage-divider rule. That is,

\[ V_i = \frac{R_i V_s}{R_i + R_s} \]  

(5.91)

Equation (5.91) clearly shows that the larger the magnitude of \( R_s \), the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system.

For the two-port system of Fig. 5.64,

\[ V_o = A_{NL} V_i \]

and

\[ V_i = \frac{R_i V_s}{R_i + R_s} \]
so that

\[ V_o = A_{vNL} \frac{R_i}{R_i + R_s} V_s \]

and

\[ A_{vj} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{vNL} \]  (5.92)

The effects of \( R_s \) and \( R_L \) have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 5.65, a source with an internal resistance \( R_s \) and a load \( R_L \) have been applied to a two-port system for which the parameters \( Z_i \), \( A_{vNL} \), and \( Z_o \) have been specified. For the moment, let us assume that \( Z_i \) and \( Z_o \) are unaffected by \( R_L \) and \( R_s \), respectively.

\[ \text{FIG. 5.65} \]

Considering the effects of \( R_s \) and \( R_L \) on the gain of an amplifier.

At the input side we find

Eq. (5.91):

\[ V_i = \frac{R_i V_s}{R_i + R_s} \]

or

\[ \frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} \]  (5.93)

and at the output side,

\[ V_o = \frac{R_L}{R_L + R_o} A_{vNL} V_i \]

or

\[ A_{vL} = \frac{V_o}{V_i} = \frac{R_i A_{vNL}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{vNL} \]  (5.94)

For the total gain \( A_{vj} = V_o/V_s \), the following mathematical steps can be performed:

\[ A_{vj} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \frac{V_i}{V_s} \]  (5.95)

and substituting Eqs. (5.93) and (5.94) results in

\[ A_{vj} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o} A_{vNL} \]  (5.96)

Because \( I_i = V_i/R_i \), as before,

\[ A_{iL} = -A_{vL} \frac{R_i}{R_L} \]  (5.97)

or, using \( I_s = V_s/(R_s + R_i) \),

\[ A_{iL} = -A_{vj} \frac{R_s + R_i}{R_L} \]  (5.98)
However, $I_i = I_s$, so Eqs. (5.97) and (5.98) generate the same result. Equation (5.96) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (5.96) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that $R_s$ is relatively small if the effect of the magnitude of $R_L$ is ignored. For instance, in Eq. (5.96), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to $(0.9)(0.2) = 0.18$, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be $(0.9)(0.9) = 0.81$, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of $R_s$ and $R_L$ must be evaluated individually and as a product.

**EXAMPLE 5.12** Determine $A_{vL}$ and $A_{vs}$ for the network of Example 5.11 and compare solutions. Example 5.1 showed that $A_{vNL} = -280$, $Z_i = 1.07 \, k\Omega$, and $Z_o = 3 \, k\Omega$. In Example 5.11, $R_L = 4.7 \, k\Omega$ and $R_s = 0.3 \, k\Omega$.

**Solution:**

a. Eq. (5.89): $A_{vL} = \frac{R_L}{R_L + R_o} A_{vNL}$

$$= \frac{4.7 \, k\Omega}{4.7 \, k\Omega + 3 \, k\Omega} (-280.11)$$

$$= -170.98$$

as in Example 5.11.

b. Eq. (5.96): $A_{vs} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{vNL}$

$$= \frac{1.07 \, k\Omega}{1.07 \, k\Omega + 0.3 \, k\Omega} \cdot \frac{4.7 \, k\Omega}{4.7 \, k\Omega + 3 \, k\Omega} (-280.11)$$

$$= (0.781)(0.610)(-280.11)$$

$$= -133.45$$

as in Example 5.11.

**EXAMPLE 5.13** Given the packaged (no-entry-possible) amplifier of Fig. 5.66:

a. Determine the gain $A_{vL}$ and compare it to the no-load value with $R_L = 1.2 \, k\Omega$.

b. Repeat part (a) with $R_L = 5.6 \, k\Omega$ and compare solutions.

c. Determine $A_{vs}$ with $R_L = 1.2 \, k\Omega$.

d. Find the current gain $A_i = \frac{I_o}{I_i} = \frac{I_o}{I_s}$ with $R_L = 5.6 \, k\Omega$.

![Diagram](image_url)
**Solution:**

a. Eq. (5.89): \( A_{vl} = \frac{R_L}{R_L + R_o} A_{vnl} \)
   \[
   = \frac{1.2 \, \text{k}\Omega}{1.2 \, \text{k}\Omega + 2 \, \text{k}\Omega} (-480) = (0.375)(-480) = -180
   \]
   which is a dramatic drop from the no-load value.

b. Eq. (5.89): \( A_{vl} = \frac{R_L}{R_L + R_o} A_{vnl} \)
   \[
   = \frac{5.6 \, \text{k}\Omega}{5.6 \, \text{k}\Omega + 2 \, \text{k}\Omega} (-480) = (0.737)(-480) = -353.76
   \]
   which clearly reveals that the larger the load resistor, the better is the gain.

c. Eq. (5.96): \( A_{vs} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{vnl} \)
   \[
   = \frac{4 \, \text{k}\Omega}{4 \, \text{k}\Omega + 0.2 \, \text{k}\Omega} \cdot \frac{1.2 \, \text{k}\Omega}{1.2 \, \text{k}\Omega + 2 \, \text{k}\Omega} (-480)
   \]
   \[
   = (0.952)(0.375)(-480) = -171.36
   \]
   which is fairly close to the loaded gain \( A_v \) because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

d. \( A_{il} = \frac{I_o}{I_i} = \frac{I_o}{I_s} = -A_{vl} \frac{Z_i}{R_L} \)
   \[
   = -(-353.76) \left( \frac{4 \, \text{k}\Omega}{5.6 \, \text{k}\Omega} \right) = -(-353.76)(0.714)
   \]
   \[
   = 252.6
   \]

It is important to realize that when using the two-port equations in some configurations the input impedance is sensitive to the applied load (such as the emitter-follower and collector feedback) and in some the output impedance is sensitive to the applied source resistance (such as the emitter-follower). In such cases the no-load parameters for \( Z_i \) and \( Z_o \) have to first be calculated before substituting into the two-port equations. For most packaged systems such as op-amps this sensitivity of the input and output parameters to the applied load or source resistance is minimized to eliminate the need to be concerned about changes from the no-load levels when using the two-port equations.

### 5.16 Cascaded Systems

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 5.67, where \( A_{v1}, A_{v2}, A_{v3}, \) and so on, are the voltage gains of each stage under loaded conditions. That is, \( A_{v1} \) is determined with the input impedance to \( A_{v2} \) acting as the load on \( A_{v1} \). For \( A_{v2}, A_{v3} \) will determine the signal strength and source impedance at the input to \( A_{v2} \). The total gain of the system is then determined by the product of the individual gains as follows:

\[
A_{vt} = A_{v1} \cdot A_{v2} \cdot A_{v3} \cdots
\]  \hspace{1cm} (5.99)

and the total current gain is given by

\[
A_{it} = -A_{vt} \frac{Z_{i1}}{R_L}
\]  \hspace{1cm} (5.100)
No matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where \( A_{v1}, A_{v2}, \) and so on, of Fig. 5.67 are simply the no-load values. The no-load parameters can be used to determine the loaded gains of each stage, but Eq. (5.99) requires the loaded values. The load on stage 1 is \( Z_i = Z_{i1} \), on stage 2 \( Z_{i2} \), on stage 3 \( Z_{i3} \), and so on.

**FIG. 5.67**
Cascaded system.

**EXAMPLE 5.14** The two-stage system of Fig. 5.68 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 5.68, the no-load values are provided for each system, with the exception of \( Z_i \) and \( Z_o \) for the emitter-follower, which are the loaded values. For the configuration of Fig. 5.68, determine:

a. The loaded gain for each stage.

b. The total gain for the system, \( A_v \) and \( A_{vs} \).

c. The total current gain for the system.

d. The total gain for the system if the emitter-follower configuration were removed.

**Solution:**

a. For the emitter-follower configuration, the loaded gain is (by Eq. (5.94))

\[
V_{o1} = \frac{Z_{i2}}{Z_{i1} + Z_{o1}} A_{vNL} V_{i1} = \frac{26 \Omega}{26 \Omega + 12 \Omega} (1) V_{i1} = 0.684 V_{i1}
\]

and

\[
A_{v1} = \frac{V_{o1}}{V_{i1}} = 0.684
\]

For the common-base configuration,

\[
V_{o2} = \frac{R_L}{R_L + R_{o2}} A_{vNL} V_{i2} = \frac{8.2 \Omega}{8.2 \Omega + 5.1 \Omega} (240) V_{i2} = 147.97 V_{i2}
\]

and

\[
A_{v2} = \frac{V_{o2}}{V_{i2}} = 147.97
\]

b. Eq. (5.99): \( A_{vs} = A_{v1} A_{v2} \)

\[
= (0.684)(147.97) = 101.20
\]
Eq. (5.91): \[ A_{v_r} = \frac{Z_{i_1}}{Z_{i_1} + R_s}A_{v_T} = \frac{(10 \, \text{k}\Omega)(101.20)}{10 \, \text{k}\Omega + 1 \, \text{k}\Omega} = 92 \]

c. Eq. (5.100): \[ A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L} = -(101.20) \left(\frac{10 \, \text{k}\Omega}{8.2 \, \text{k}\Omega}\right) = -123.41 \]
d. Eq. (5.91): \[ V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s}V_s = \frac{26 \, \Omega}{26 \, \Omega + 1 \, \text{k}\Omega}V_s = 0.025V_s \]

and \[ \frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above} \]

and \[ A_{v_i} = \frac{V_o}{V_i} = \frac{V_o}{V_i} = \frac{0.025}{147.97} = 3.7 \]

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been “lost” again by the voltage-divider action.

**RC-Coupled BJT Amplifiers**

One popular connection of amplifier stages is the RC-coupled variety shown in Fig. 5.69 in the next example. The name is derived from the capacitive coupling capacitor \( C_C \) and the fact that the load on the first stage is an RC combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

**EXAMPLE 5.15**

a. Calculate the no-load voltage gain and output voltage of the RC-coupled transistor amplifiers of Fig. 5.69.
b. Calculate the overall gain and output voltage if a 4.7 k\( \Omega \) load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

**Solution:**
a. The dc bias analysis results in the following for each transistor:
\[ V_B = 4.8 \, \text{V}, \quad V_E = 4.1 \, \text{V}, \quad V_C = 11 \, \text{V}, \quad I_E = 4.1 \, \text{mA} \]
At the bias point,

\[ r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{4.1 \text{ mA}} = 6.34 \Omega \]

The loading of the second stage is

\[ Z_{i2} = R_1 \parallel R_2 \beta r_e \]

which results in the following gain for the first stage:

\[ A_{v1} = \frac{R_C \parallel (R_1 \parallel R_2 \beta r_e)}{r_e} = \frac{(2.2 \text{ k}\Omega \parallel [15 \text{ k}\Omega \parallel 4.7 \text{ k}\Omega \parallel (200)(6.34 \Omega)]}{6.34 \Omega} = \frac{659.2 \Omega}{6.34 \Omega} = -104 \]

For the unloaded second stage the gain is

\[ A_{v2(NL)} = -\frac{R_C}{r_e} = -\frac{2.2 \text{ k}\Omega}{6.34 \Omega} = -347 \]

resulting in an overall gain of

\[ A_{vT(NL)} = A_{v1}A_{v2(NL)} = (-104)(-347) \approx 36.1 \times 10^3 \]

The output voltage is then

\[ V_o = A_{vT(NL)}V_i = (36.1 \times 10^3)(25 \mu\text{V}) \approx 902.5 \text{ mV} \]

b. The overall gain with the 10-k\Omega load applied is

\[ A_{vT} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o A_{vT(NL)}} = \frac{4.7 \text{ k}\Omega}{4.7 \text{ k}\Omega + 2.2 \text{ k}\Omega (36.1 \times 10^3)} \approx 24.6 \times 10^3 \]

which is considerably less than the unloaded gain because \( R_L \) is relatively close to \( R_C \):

\[ V_o = A_{vT}V_i = (24.6 \times 10^3)(25 \mu\text{V}) = 615 \text{ mV} \]

c. The input impedance of the first stage is

\[ Z_{i1} = R_1 \parallel R_2 \beta r_e = 4.7 \text{ k}\Omega \parallel 15 \text{ k}\Omega \parallel (200)(6.34 \Omega) = 0.94 \text{ k}\Omega \]

whereas the output impedance for the second stage is

\[ Z_{o2} = R_C = 2.2 \text{ k}\Omega \]

**Cascode Connection**

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.70; the second is shown in Fig. 5.71 in the following example.

![FIG. 5.70 Cascode configuration.](image)
The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance (to be discussed in Section 9.9) is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

**EXAMPLE 5.16** Calculate the no-load voltage gain for the cascode configuration of Fig. 5.71.

\[
V_{CC} = 18 \text{ V} \\
V_{i1} = 4.9 \text{ V}, \quad V_{B1} = 10.8 \text{ V}, \quad I_{C1} \approx I_{C2} = 3.8 \text{ mA}
\]

because \( I_{E1} \approx I_{E2} \) the dynamic resistance for each transistor is

\[
r_e = \frac{26 \text{ mV}}{3.8 \text{ mA}} = 6.8 \Omega
\]

The loading on the transistor \( Q_1 \) is the input impedance of the \( Q_2 \) transistor in the CB configuration as shown by \( r_e \) in Fig. 5.72.

The result is the replacement of \( R_C \) in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

\[
A_{v1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1
\]

with the voltage gain for the second stage (common base) of

\[
A_{v2} = \frac{R_C}{r_e} = \frac{1.8 \text{ k}\Omega}{6.8 \Omega} = 265
\]
The overall no-load gain is

\[ A_{\text{V}} = A_{v1}A_{v2} = (-1)(265) = -265 \]

As expected, in Example 5.16, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.

### 5.17 DARLINGTON CONNECTION

A very popular connection of two bipolar junction transistors for operation as one “super-beta” transistor is the Darlington connection shown in Fig. 5.73. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of \( \beta_1 \) and \( \beta_2 \), the Darlington connection provides a current gain of

\[ \beta_D = \beta_1\beta_2 \]  \hspace{1cm} (5.101)

![FIG. 5.73 Darlington combination.](image)

The configuration was first introduced by Dr. Sidney Darlington in 1953. A short biography appears as Fig 5.74.

**Emitter-Follower Configuration**

A Darlington amplifier used in an emitter-follower configuration appears in Fig. 5.75. The primary impact of using the Darlington configuration is an input impedance much larger than

![FIG. 5.75 Emitter-follower configuration with a Darlington amplifier.](image)
that obtained with a single-transistor network. The current gain is also larger, but the voltage gain for a single-transistor or Darlington configuration remains slightly less than one.

**DC Bias** The case current is determined using a modified version of Eq. 4.44. There are now two base-to-emitter voltage drops to include and the beta of a single transistor is replaced by the Darlington combination of Eq. 5.101.

\[
I_{B1} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_B + \beta_D R_E}
\]  
(5.102)

The emitter current of \( Q_1 \) is equal to the base current of \( Q_2 \) so that

\[
I_{E2} = \beta_2 I_{B2} = \beta_2 I_{E1} = \beta_2 (\beta_1 I_{E1}) = \beta_1 \beta_2 I_{B1}
\]
resulting in

\[
I_{C2} = I_{E2} = \beta_D I_{B1}
\]  
(5.103)

The collector voltage of both transistors is

\[
V_{C1} = V_{C2} = V_{CC}
\]  
(5.104)

the emitter voltage of \( Q_2 \)

\[
V_{E2} = I_{E2} R_E
\]  
(5.105)

the base voltage of \( Q_1 \)

\[
V_{B1} = V_{CC} - I_{B2} R_B = V_{E2} + V_{BE1} + V_{BE2}
\]  
(5.106)

the collector-emitter voltage of \( Q \)

\[
V_{CE2} = V_{C2} - V_{E2} = V_{CC} - V_{E2}
\]  
(5.107)

**EXAMPLE 5.17** Calculate the dc bias voltages and currents for the Darlington configuration of Fig. 5.76.

\[+18 \text{ V}\]

\[3.3 \text{ M\Omega}\]

\[V_i\]

\[\beta_1 = 50\]

\[\beta_2 = 100\]

\[390 \Omega\]

\[V_o\]

**FIG. 5.76** Circuit for Example 5.17.
**Solution:**

\[ \beta_D = \beta_1 \beta_2 = (50)(100) = 5000 \]

\[ I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} = \frac{18 \text{ V} - 0.7 \text{ V} - 0.7 \text{ V}}{3.3 \text{ MΩ} + (5000)(390 \text{ Ω})} \]

\[ = \frac{18 \text{ V} - 1.4 \text{ V}}{3.3 \text{ MΩ} + 1.95 \text{ MΩ}} = \frac{16.6 \text{ V}}{5.25 \text{ MΩ}} = 3.16 \text{ μA} \]

\[ I_{C_2} \equiv I_{E_2} = \beta_D I_{B_1} = (5000)(3.16 \text{ mA}) = 15.80 \text{ mA} \]

\[ V_{C_1} = V_{C_2} = 18 \text{ V} \]

\[ V_{E_2} = I_{E_2} R_E = (15.80 \text{ mA})(390 \text{ Ω}) = 6.16 \text{ V} \]

\[ V_{B_1} = V_{E_2} + V_{BE_1} + V_{BE_2} = 6.16 \text{ V} + 0.7 \text{ V} + 0.7 \text{ V} = 7.56 \text{ V} \]

\[ V_{CE_2} = V_{CC} - V_{E_2} = 18 \text{ V} - 6.16 \text{ V} = 11.84 \text{ V} \]

**AC Input Impedance** The ac input impedance can be determined using the ac equivalent network of Fig. 5.77.

![Diagram](image)

As defined in Fig. 5.77:

\[ Z_i = \beta_2 (r_e_2 + R_E) \]

\[ Z_i = \beta_1 (r_e_1 + Z_{i_2}) \]

so that

\[ Z_{i_1} = \beta_1 (r_e_1 + \beta_2 (r_e_2 + R_E)) \]

Assuming

\[ R_E \gg r_e \]

and

\[ Z_{i_1} = \beta_1 (r_e_1 + \beta_2 R_E) \]

Since

\[ \beta_2 R_E \gg r_e_1 \]

\[ Z_{i_1} \equiv \beta_1 \beta_2 R_E \]

and since

\[ Z_i = R_B \parallel Z_{i_1} \]

For the network of Fig. 5.76

\[ Z_i = R_B \parallel \beta_D R_E \]

\[ = 3.3 \text{ MΩ} \parallel (5000)(390 \text{ Ω}) = 3.3 \text{ MΩ} \parallel 1.95 \text{ MΩ} \]

\[ = 1.38 \text{ MΩ} \]

Note in the preceding analysis that the values of \(r_e\) were not compared but dropped compared to much larger quantities. In a Darlington configuration the values of \(r_e\) will be different because the emitter current through each transistor will be different. Also, keep in mind that chances are the beta values for each transistor will be different because they deal with different current levels. The fact remains, however, that the product of the two beta values will equal \(\beta_D\), as indicated on the specification sheet.
**AC Current Gain** The current gain can be determined from the equivalent network of Fig. 5.78. The output impedance of each transistor is ignored and the parameters for each transistor are employed.

![Diagram of BJT AC Analysis](image)

**FIG. 5.78**

Determining $A_i$ for the network of Fig. 5.75.

Solving for the output current: $I_o = I_{b2} + \beta_2 I_{b6} = (\beta_2 + 1)I_{b6}$

with $I_{b2} = \beta_1 I_{b1} + I_{b1} = (\beta_1 + 1)I_{b1}$

Then $I_o = (\beta_2 + 1)(\beta_1 + 1)I_{b1}$

Using the current-divider rule on the input circuit:

$I_{b1} = \frac{R_B}{R_B + Z_i} I_i = \frac{R_B}{R_B + \beta_1 \beta_2 R_E} I_i$

and

$I_o = (\beta_2 + 1)(\beta_1 + 1)\left(\frac{R_B}{R_B + \beta_1 \beta_2 R_E}\right)I_i$

so that

$A_i = \frac{I_o}{I_i} = \frac{(\beta_1 + 1)(\beta_2 + 1)R_B}{R_B + \beta_1 \beta_2 R_E}$

Using $\beta_1, \beta_2 \gg 1$

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_E} \quad (5.109)$$

or

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta_D R_B}{R_B + \beta_D R_E} \quad (5.110)$$

For Fig. 5.76:

$$A_i = \frac{I_o}{I_i} = \frac{\beta_D R_B}{R_B + \beta_D R_E} = \frac{(5000)(3.3 \, \text{M}\Omega)}{3.3 \, \text{M}\Omega + 1.95 \, \text{M}\Omega}$$

$$= 3.14 \times 10^3$$

**AC Voltage Gain** The voltage gain can be determined using Fig. 5.77 and the following derivation:

$$V_o = I_o R_E$$

$$V_i = I_i (R_B || Z_i)$$

$$R_B || Z_i = R_B || \beta_D R_E = \frac{\beta_D R_B R_E}{R_B + \beta_D R_E}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{I_o R_E}{I_i (R_B || Z_i)} = (A_i) \left( \frac{R_E}{R_B || Z_i} \right)$$

$$= \left[ \frac{\beta_D R_B}{R_B + \beta_D R_E} \right] \left[ \frac{R_E}{\beta_D R_B R_E} \right]$$

and

$$A_v \approx 1 \text{ (in reality less than one)} \quad (5.111)$$

an expected result for the emitter-follower configuration.
AC Output Impedance  
The output impedance will be determined by going back to Fig. 5.78 and setting $V_i$ to zero volts as shown in Fig. 5.79. The resistor $R_B$ is “shorted out,” resulting in the configuration of Fig. 5.80. Note in Figs. 5.82 and 5.83 that the output current has been redefined to match standard nomenclature and properly defined $Z_o$.

**FIG. 5.79**
Determining $Z_o$

**FIG. 5.80**
Redrawn of network of Fig. 5.79.

At point $a$ Kirchhoff’s current law will result in $I_o + (\beta_2 + 1)I_{b2} = I_e$:

$$I_o = I_e - (\beta_2 + 1)I_{b2}$$

Applying Kirchhoff’s voltage law around the entire outside loop will result in

$$-I_{b2}\beta_1 r_{e1} - I_{b2}\beta_2 r_{e2} - V_o = 0$$

and

$$V_o = I_{b2}\beta_1 r_{e1} + I_{b2}\beta_2 r_{e2}$$

Substituting $I_{b2} = (\beta_1 + 1)I_{b1}$

$$V_o = -I_{b2}\beta_1 r_{e1} - (\beta_1 + 1)I_{b2}\beta_2 r_{e2} = -I_{b1}[\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}]$$

and

$$I_{b1} = -\frac{V_o}{\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}}$$

with

$$I_{b2} = (\beta_1 + 1)I_{b1} = (\beta_1 + 1)\left[-\frac{V_o}{\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}}\right]$$

so that

$$I_{b2} = -\left[\frac{\beta_1 + 1}{\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}}\right]V_o$$

Going back

$$I_o = I_e - (\beta_2 + 1)I_{b2} = I_e - (\beta_2 + 1)\left[-\frac{(\beta_1 + 1)V_o}{\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}}\right]$$

or

$$I_o = \frac{V_o}{R_E} + \frac{(\beta_1 + 1)(\beta_2 + 1)V_o}{\beta_1 r_{e1} + (\beta_1 + 1)\beta_2 r_{e2}}$$
Because $\beta_1, \beta_2 \gg 1$

\[
I_o = \frac{V_o}{R_E} + \frac{\beta_1 \beta_2 V_o}{\beta_1 r_e_1 + \beta_1 \beta_2 r_e_2} = \frac{V_o}{R_E} + \frac{V_o}{\beta_1 r_e_1 + \beta_1 \beta_2 r_e_2}
\]

\[
I_o = \frac{V_o}{R_E} + \frac{V_o}{\beta_1 r_e_1 + \beta_1 \beta_2 r_e_2}
\]

which defines the parallel resistance network of Fig. 5.81.

In general, $R_E \gg \left(\frac{r_e_1}{\beta_2} + r_e_2\right)$ so the output impedance is defined by

\[
Z_o = \frac{r_e_1}{\beta_2} + r_e_2
\]

(5.112)

Using the dc results, the value of $r_e_2$ and $r_e_1$ can be determined as follows.

\[
r_e_2 = \frac{26 \text{ mV}}{15.80 \text{ mA}} = 1.65 \Omega
\]

and

\[
I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{15.80 \text{ mA}}{100} = 0.158 \text{ mA}
\]

so that

\[
r_e_1 = \frac{26 \text{ mV}}{0.158 \text{ mA}} = 164.5 \Omega
\]

The output impedance for the network of Fig. 5.78 is therefore:

\[
Z_o \equiv \frac{r_e_1}{\beta_2} + r_e_2 = \frac{164.5 \Omega}{100} + 1.65 \Omega = 1.645 \Omega + 1.65 \Omega = 3.30 \Omega
\]

In general, the output impedance for the configuration of Fig. 5.78 is very low—in the order of a few ohms at most.

**Voltage-Divider Amplifier**

**DC Bias** Let us now investigate the effect of the Darlington configuration in a basic amplifier configuration as shown in Fig. 5.82. Note that now there is a collector resistor $R_C$, and the emitter terminal of the Darlington circuit is connected to ground for ac conditions. As noted on Fig. 5.82, the beta of each transistor is provided along with the resulting voltage from base to emitter.
The dc analysis can proceed as follows:

\[ \beta_D = \beta_1 \beta_2 = (110 \times 110) = 12,100 \]

\[ V_B = \frac{R_2}{R_2 + R_1} V_{CC} = \frac{220 \text{k}\Omega(27 \text{ V})}{220 \text{k}\Omega + 470 \text{k}\Omega} = 8.61 \text{ V} \]

\[ V_E = V_B - V_{BE} = 8.61 \text{ V} - 1.5 \text{ V} = 7.11 \text{ V} \]

\[ I_E = \frac{V_E}{R_E} = \frac{7.11 \text{ V}}{680 \text{ } \Omega} = 10.46 \text{ mA} \]

\[ I_B = \frac{I_E}{\beta_D} = \frac{10.46 \text{ mA}}{12,100} = 0.864 \mu\text{A} \]

Using the preceding results the values of \( r_{e_2} \) and \( r_{e_1} \) can be determined:

\[ r_{e_2} = \frac{26 \text{ mV}}{I_{E_2}} = \frac{26 \text{ mV}}{10.46 \text{ mA}} = 2.49 \text{ } \Omega \]

\[ I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{10.46 \text{ mA}}{110} = 0.095 \text{ mA} \]

and

\[ r_{e_1} = \frac{26 \text{ mV}}{I_{E_1}} = \frac{26 \text{ mV}}{0.095 \text{ mA}} = 273.7 \text{ } \Omega \]

**AC Input Impedance** The ac equivalent of Fig. 5.82 appears as Fig. 5.83. The resistors \( R_1 \) and \( R_2 \) are in parallel with the input impedance to the Darlington pair, assuming the second transistor found by assuming the second transistor acts like an \( R_E \) load on the first as shown in Fig. 5.83.

That is, \( Z'_i = \beta_1 r_{e_1} + \beta_1 (\beta_2 r_{e_2}) \)

\[ Z'_i = \beta_1 [r_{e_1} + \beta_2 r_{e_2}] \] (5.113)

For the network of Fig. 5.82:

\[ Z'_i = 110[(273.7 \text{ } \Omega + (110)(2.49 \text{ } \Omega))] \]

\[ = 110[273.7 \text{ } \Omega + 273.9 \text{ } \Omega] \]

\[ = 110[547.6 \text{ } \Omega] \]

\[ = 60.24 \text{ k}\Omega \]

and

\[ Z_i = R_1 \| R_2 \| Z'_i \]

\[ = 470 \text{ k}\Omega \| 220 \text{ k}\Omega \| 60.24 \text{ k}\Omega \]

\[ = 149.86 \text{ k}\Omega \] (60.24 k\Omega)

\[ = 42.97 \text{ k}\Omega \]
**AC Current Gain**  The complete ac equivalent of Fig. 5.82 appears as Fig. 5.84.

The output current

\[ I_o = \beta_1 I_{b1} + \beta_2 I_{b2} \]

with

\[ I_{b2} = (\beta_1 + 1) I_{b1} \]

so that

\[ I_o = \beta_1 I_{b1} + \beta_2 (\beta_1 + 1) I_{b1} \]

and with

\[ I_{b1} = I' \]

we find

\[ I_o = \beta_1 I' + \beta_2 (\beta_1 + 1) I' \]

and

\[ A'_i = \frac{I'_o}{I'_i} = \beta_1 + \beta_2 (\beta + 1) \]

\[ \equiv \beta_1 + \beta_2 \beta_1 = \beta_1 (1 + \beta_2) \]

\[ \equiv \beta_1 \beta_2 \]

and finally

\[ A'_i = \frac{I'_o}{I'_i} = \beta_1 \beta_2 = \beta_D \]  \hspace{1cm} (5.114)

For the original structure:

\[ I'_i = \frac{R_1 \| R_2 I_i}{R_1 \| R_2 + Z'_i} \quad \text{or} \quad \frac{I'_i}{I_i} = \frac{R_1 \| R_2}{R_1 \| R_2 + Z'_i} \]

but

\[ A_i = \frac{I_o}{I_i} = \left( \frac{I'_o}{I'_i} \right) \left( \frac{I'_i}{I_i} \right) \]

so that

\[ A_i = \frac{\beta_D (R_1 \| R_2)}{R_1 \| R_2 + Z'_i} \]  \hspace{1cm} (5.115)

For Fig. 5.82

\[ A_i = \frac{(12,100)(149.86 \, \text{k}\Omega)}{149.86 \, \text{k}\Omega + 60.24 \, \text{k}\Omega} = 8630.7 \]

Note the significant drop in current gain due to \( R_1 \) and \( R_2 \).

**AC Voltage Gain**  The input voltage is the same across \( R_1 \) and \( R_2 \) and at the base of the first transistor as shown in Fig. 5.84.

The result is

\[ A_v = \frac{V_o}{V_i} = -\frac{I_o R_C}{I'_i Z'_i} = -A_i \left( \frac{R_C}{Z'_i} \right) \]

and

\[ A_v = -\frac{\beta_D R_C}{Z'_i} \]  \hspace{1cm} (5.116)

For the network of Fig. 5.82,

\[ A_v = -\frac{(12,000)(1.2 \, \text{k}\Omega)}{60.24 \, \text{k}\Omega} = -241.04 \]
AC Output Impedance Because the output impedance in \( R_C \) is parallel with the collector to emitter terminals of the transistor, we can look back on similar situations and find that the output impedance is defined by

\[
Z_o \approx R_C \| r_o2
\]

(5.117)

where \( r_o2 \) is the output resistance of the transistor \( Q_2 \).

Packaged Darlington Amplifier

Because the Darlington connection is so popular, a number of manufacturers provide packaged units such as shown in Fig. 5.85. Typically, the two BJTs are constructed on a single chip rather than separate BJT units. Note that only one set of collector, base, and emitter terminals is provided for each configuration. These, of course, are the base of the transistor \( Q_1 \), the collector of \( Q_1 \) and \( Q_2 \), and the emitter of \( Q_2 \).

![Fig. 5.85](image)

In Fig. 5.86 some of the ratings for an MPSA28 Fairchild Semiconductor Darlington amplifier are provided. In particular, note that the maximum collector-to-emitter voltage of 80 V is also the breakdown voltage. The same is true for the collector-to-base and emitter-to-base voltages, although notice how much lower the maximum ratings are for the base-to-emitter junction. Because of the Darlington configuration, the maximum current rating for the collector current has jumped to 800 mA—far exceeding levels we have encountered before.

### Absolute Maximum Ratings

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<th>Parameter</th>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>( V_{CES} )</td>
<td>Collector-Emitter Voltage</td>
<td>80 V</td>
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<tr>
<td>( V_{CBO} )</td>
<td>Collector-Base Voltage</td>
<td>80 V</td>
</tr>
<tr>
<td>( V_{EBO} )</td>
<td>Emitter-Base Voltage</td>
<td>12 V</td>
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<tr>
<td>( I_C )</td>
<td>Collector Current—Continuous</td>
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### Electrical Characteristics

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<td>( V_{(BR)CES} )</td>
<td>Collector-Emitter Breakdown Voltage</td>
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<tr>
<td>( V_{(BR)CBO} )</td>
<td>Collector-Base Breakdown Voltage</td>
<td>80 V</td>
</tr>
<tr>
<td>( V_{(BR)EBO} )</td>
<td>Emitter-Base Breakdown Voltage</td>
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<tr>
<td>( I_{CBO} )</td>
<td>Collector Cutoff Current</td>
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</tr>
<tr>
<td>( I_{EBO} )</td>
<td>Emitter Cutoff Current</td>
<td>100 mA</td>
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### On Characteristics

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<td>( V_{CE(sat)} )</td>
<td>Collector-Emitter Saturation Voltage</td>
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<tr>
<td>( V_{BE(on)} )</td>
<td>Base-Emitter on Voltage</td>
<td>2.0 V</td>
</tr>
</tbody>
</table>

![Fig. 5.86](image)
BJT AC ANALYSIS

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for single-transistor networks. The dc current gain is rated at the high level of 10,000 and the base-to-emitter potential in the “on” state is 2 V, which certainly exceeds the 1.4 V we have used for individual transistors. Finally, it is interesting to note that the level of $I_{CEO}$ is much higher at 500 nA than for a typical single-transistor unit.

In the packaged format the network of Fig. 5.75 would appear as shown in Fig. 5.87. Using $\beta_D$ and the provided value of $V_{BE} (= V_{BE_1} + V_{BE_2})$, all the equations appearing in this section can be applied.

The feedback pair connection (see Fig. 5.88) is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a $pnp$ transistor driving an $npn$ transistor, the two devices acting effectively much like one $pnp$ transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains), high input impedance, low output impedance, and a voltage gain slightly less than one. Initially, it may appear that it would have a high voltage gain because the output is taken off the collector with a resistor $R_C$ in place. However, the $pnp$–$npn$ combination results in terminal characteristics very similar to that of the emitter–follower configuration. A typical application (see Chapter 12) uses a Darlington and a feedback-pair connection to provide complementary transistor operation. A practical network employing a feedback pair is provided in Fig. 5.89 for investigation.

**DC Bias**

The dc bias calculations that follow use practical simplifications wherever possible to provide simpler results. From the $Q_1$ base–emitter loop, one obtains

$$V_{CC} - I_C R_C - V_{EB_1} - I_B R_B = 0$$

$$V_{CC} - (\beta_1 \beta_2 I_B) R_C - V_{EB_1} - I_B R_B = 0$$

The base current is then

$$I_{B_1} = \frac{V_{CC} - V_{BE_1}}{R_B + \beta_1 \beta_2 R_C} \quad (5.118)$$

The collector current of $Q_1$ is

$$I_{C_1} = \beta_1 I_{B_1} = I_{B_2}$$

which is also the base $Q_2$ current. The transistor $Q_2$ collector current is

$$I_{C_2} = \beta_2 I_{B_2} = I_{E_2}$$
so that the current through $R_C$ is

$$I_C = I_{E_1} + I_{C_2} = I_{B_1} + I_{C_2} \quad (5.119)$$

The voltages

$$V_{C_2} = V_{E_1} = V_{CC} - I_C R_C \quad (5.120)$$

and

$$V_{B_1} = I_{B_1} R_B \quad (5.121)$$

with

$$V_{BC_1} = V_{B_1} - V_{BE_2} = V_{B_1} - 0.7 \text{ V} \quad (5.122)$$

**EXAMPLE 5.18**  Calculate the dc bias currents and voltages for the circuit of Fig. 5.89 to provide $V_o$ at one-half the supply voltage (9 V).

**Solution:**

$$I_{B_1} = \frac{18 \text{ V} - 0.7 \text{ V}}{2 \text{ M} \Omega + (140)(180)(75 \text{ } \Omega)} = \frac{17.3 \text{ V}}{3.89 \times 10^6} = 4.45 \mu\text{A}$$

The base $Q_2$ current is then

$$I_{B_2} = I_{C_1} = \beta_{1} I_{B_1} = 140(4.45 \mu\text{A}) = 0.623 \text{ mA}$$

resulting in a $Q_2$ collector current of

$$I_{C_2} = \beta_{2} I_{B_2} = 180(0.623 \text{ mA}) = 112.1 \text{ mA}$$

and the current through $R_C$ is then

Eq. (5.119): $I_C = I_{E_1} + I_{C_2} = 0.623 \text{ mA} + 112.1 \text{ mA} = I_{C_2} = 112.1 \text{ mA}$

$$V_{C_2} = V_{E_1} = 18 \text{ V} - (112.1 \text{ mA})(75 \text{ } \Omega)$$

$$= 18 \text{ V} - 8.41 \text{ V}$$

$$= 9.59 \text{ V}$$

$$V_{B_1} = I_{B_1} R_B = (4.45 \mu\text{A})(2 \text{ M} \Omega)$$

$$= 8.9 \text{ V}$$

$$V_{BC_1} = V_{B_1} - 0.7 \text{ V} = 8.9 \text{ V} - 0.7 \text{ V}$$

$$= 8.2 \text{ V}$$
**AC Operation**

The ac equivalent circuit for that of Fig. 5.89 is drawn in Fig. 5.90.

![AC equivalents circuit](image)

**FIG. 5.90**
ac equivalent for the network of Fig. 5.89.

**Input Impedance, $Z_i$**  The ac input impedance seen looking into the base of transistor $Q_1$ is determined as follows:

$$Z'_i = \frac{V_i}{I'_i}$$

Applying Kirchhoff’s current law at node $a$ and defining $I_c = I_o$:

$$I_{b1} + \beta_1 I_{b1} - \beta_2 I_{b2} + I_o = 0$$

with $I_{b2} = -\beta_1 I_{b1}$ as noted in Fig. 5.90.

The result is

$$I_{b1} + \beta_1 I_{b1} - \beta_2(-\beta_1 I_{b1}) + I_o = 0$$

and

$$I_o = -I_{b1} - \beta_1 I_{b1} - \beta_1 \beta_2 I_{b1}$$

or

$$I_o = -I_{b1}(1 + \beta_1) - \beta_1 \beta_2 I_{b1}$$

but

$$\beta_1 \gg 1$$

and

$$I_o = -\beta_1 I_{b1} - \beta_1 \beta_2 I_{b1} = -I_{b1}(\beta_1 + \beta_1 \beta_2)$$

$$= -I_{b1}\beta_1(1 + \beta_2)$$

resulting in:

$$I_o \approx -\beta_1 \beta_2 I_{b1}$$  \hspace{1cm} (5.123)

Now, $I_{b1} = \frac{V_i - V_o}{\beta_1 r_{e1}}$ from Fig. 5.90

and

$$V_o = -I_o R_C = -(-\beta_1 \beta_2 I_{b1}) R_C = \beta_1 \beta_2 I_{b1} R_C$$

so

$$I_{b1} = \frac{V_i - \beta_1 \beta_2 I_{b1} R_C}{\beta_1 r_{e1}}$$

Rearranging:

$$I_{b1} r_{e1} = V_i - \beta_1 \beta_2 R_C$$

and

$$I_{b1}(\beta_1 r_{e1} + \beta_1 \beta_2 R_C) = V_i$$

so

$$I_{b1} = I'_1 = \frac{V_i}{\beta_1 r_{e1} + \beta_1 \beta_2 R_C}$$

and

$$V'_1 = \frac{V_i}{I'_1} = \frac{V_i}{\frac{V_i}{\beta_1 r_{e1} + \beta_1 \beta_2 R_C}}$$

so that

$$Z'_i = \beta_1 r_{e1} + \beta_1 \beta_2 R_C$$  \hspace{1cm} (5.124)

In general,

$$\beta_1 \beta_2 R_C \gg \beta_1 r_{e1}$$

and

$$Z'_i \approx \beta_1 \beta_2 R_C$$  \hspace{1cm} (5.125)
with

$$Z_i = R_B[Z_i']$$  \hspace{1cm} (5.126)

For the network of Fig. 5.89:

$$r_{e_1} = \frac{26 \text{ mV}}{I_{E_1}} = \frac{26 \text{ mV}}{0.623 \text{ mA}} = 41.73 \Omega$$

and

$$Z_i' = \beta_1 r_{e_1} + \beta_1 \beta_2 R_C$$

$$= (140)(41.73 \Omega) + (140)(180)(75 \Omega)$$

$$= 5842.2 \Omega + 1.89 \text{ M}\Omega$$

$$= 1.895 \text{ M}\Omega$$

where Eq. (5.125) results in

$$Z_i' = \beta_1 \beta_2 R_C = (140)(180)(75 \Omega) = 1.89 \text{ M}\Omega$$, validating

the above approximations.

**Current Gain**

Defining $I_{b_1} = I_i'$ as shown in Fig. 5.90 will permit finding the current gain $A_i' = I_o/I_i'$.

Looking back on the derivation of $Z_i$ we found $I_o = -\beta_1 \beta_2 I_{b_1} = -\beta_1 \beta_2 I_i'$

resulting in

$$A_i' = \frac{I_o}{I_i'} = -\beta_1 \beta_2$$  \hspace{1cm} (5.127)

The current gain $A_i = I_o/I_i$ can be determined using the fact that

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_i} \cdot \frac{I_i}{I_i}$$

For the input side:

$$I_i' = \frac{R_B I_i}{R_B + Z_i'}$$

Substituting:

$$A_i = \frac{I_o}{I_i} \cdot \frac{I_i'}{I_i} = (-\beta_1 \beta_2) \left( \frac{R_B}{R_B + \beta_1 \beta_2 R_C} \right)$$

So that

$$A_i = \frac{I_o}{I_i} = \frac{-\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_C}$$  \hspace{1cm} (5.128)

The negative sign appears because both $I_i$ and $I_o$ are defined as entering the network.

For the network of Fig. 5.89:

$$A_i' = \frac{I_o}{I_i'} = -\beta_1 \beta_2$$

$$= -(140)(180)$$

$$= -25.2 \times 10^3$$

$$A_i = \frac{-\beta_1 \beta_2 R_B}{R_B + \beta_1 \beta_2 R_C} = \frac{(140)(180)(2 \text{ M}\Omega)}{2 \text{ M}\Omega + 1.89 \text{ M}\Omega}$$

$$= \frac{50,400 \text{ M}\Omega}{3.89 \text{ M}\Omega}$$

$$= -12.96 \times 10^3 (\approx \text{ half of } A_i')$$

**Voltage Gain**

The voltage gain can quickly be determined using the results obtained above.

That is,

$$A_v = \frac{V_o}{V_i} = \frac{-I_o R_C}{I_i' Z_i'}$$

$$= - \frac{(-\beta_1 \beta_2 I_i') R_C}{I_i' (\beta_1 r_{e_1} + \beta_1 \beta_2 R_C)}$$

$$A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C}$$  \hspace{1cm} (5.129)
which is simply the following if we apply the approximation: \( \beta_2 R_C \gg r_{e1} \)

\[
A_v \approx \frac{\beta_2 R_C}{\beta_2 R_C} = 1
\]

For the network of Fig. 5.89:

\[
A_v = \frac{\beta_2 R_C}{r_{e1} + \beta_2 R_C} = \frac{(180)(75 \, \Omega)}{41.73 \, \Omega + (180)(75 \, \Omega)}
\]

\[
= \frac{41.73 \, \Omega + 13.5 \times 10^3 \, \Omega}{13.5 \times 10^3 \, \Omega}
\]

\[
= 0.997 \approx 1 \text{ (as indicated above)}
\]

**Output Impedance**

The output impedance \( Z_o \) is defined in Fig. 5.91 when \( V_i \) is set to zero volts.

![FIG. 5.91 Determining \( Z'_o \) and \( Z_o \)](image)

Using the fact that \( I_o = -\beta_1 \beta_2 I_{b1} \) from calculations above, we find that

\[
Z'_o = \frac{V_o}{I_o} = -\frac{V_o}{\beta_1 \beta_2 I_{b1}}
\]

but

\[
I_{b1} = -\frac{V_o}{\beta_1 r_{e1}}
\]

and

\[
Z'_o = \frac{V_o}{-\beta_1 \beta_2 \left( \frac{V_o}{\beta_1 r_{e1}} \right)} = \frac{\beta_1 r_{e1}}{\beta_1 \beta_2}
\]

so that

\[
Z'_o = \frac{r_{e1}}{\beta_2}
\]  \hspace{1cm} (5.130)

with

\[
Z_o = R_C \left( \frac{r_{e1}}{\beta_2} \right)
\]  \hspace{1cm} (5.131)

However,

\[
R_C \gg \frac{r_{e1}}{\beta_2}
\]

leaving

\[
Z_o \approx \frac{r_{e1}}{\beta_2}
\]  \hspace{1cm} (5.132)

which will be a very low value.

For the network of Fig. 5.89:

\[
Z_o \approx \frac{41.73 \, \Omega}{180} = 0.23 \, \Omega
\]

The preceding analysis shows that the feedback pair connection of Fig. 5.89 provides operation with voltage gain very near 1 (just as with a Darlington emitter-follower), a very high current gain, a very low output impedance, and a high input impedance.
The hybrid equivalent model was mentioned in the earlier sections of this chapter as one that was used in the early years before the popularity of the $r_e$ model developed. Today there is a mix of usage depending on the level and direction of the investigation.

**The $r_e$ model has the advantage that the parameters are defined by the actual operating conditions,**

whereas

**the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.**

In other words, the hybrid parameters may not reflect the actual operating conditions but simply provide an indication of the level of each parameter to expect for general use. The $r_e$ model suffers from the fact that parameters such as the output impedance and the feedback elements are not available, whereas the hybrid parameters provide the entire set on the specification sheet. In most cases, if the $r_e$ model is employed, the investigator will simply examine the specification sheet to have some idea of what the additional elements might be. This section will show how one can go from one model to the other and how the parameters are related. Because all specification sheets provide the hybrid parameters and the model is still extensively used, it is important to be aware of both models. The hybrid parameters as shown in Fig. 5.92 are derived from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

<table>
<thead>
<tr>
<th>Input impedance ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)</th>
<th>$h_{ie}$</th>
<th>Min.</th>
<th>Max.</th>
<th>kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage feedback ratio ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)</td>
<td>$h_{ie}$</td>
<td>0.5</td>
<td>7.5</td>
<td>kΩ</td>
</tr>
<tr>
<td>Small-signal current gain ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)</td>
<td>$h_{fe}$</td>
<td>0.1</td>
<td>8.0</td>
<td>$\times 10^{-4}$</td>
</tr>
<tr>
<td>Output admittance ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)</td>
<td>$h_{ce}$</td>
<td>20</td>
<td>250</td>
<td>—</td>
</tr>
</tbody>
</table>

**FIG. 5.92**

*Hybrid parameters for the 2N4400 transistor.*

The description of the hybrid equivalent model will begin with the general two-port system of Fig. 5.93. The following set of equations (5.131) and (5.132) is only one of a number of ways in which the four variables of Fig. 5.93 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.

**FIG. 5.93**

*Two-port system.*
The parameters relating the four variables are called *h-parameters*, from the word “hybrid.” The term *hybrid* was chosen because the mixture of variables (V and I) in each equation results in a “hybrid” set of units of measurement for the *h*-parameters. A clearer understanding of what the various *h*-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

**h**<sub>11</sub> If we arbitrarily set *V*<sub>o</sub> = 0 (short circuit the output terminals) and solve for *h*<sub>11</sub> in Eq. (5.133), we find

\[
 h_{11} = \left. \frac{V_i}{I_i} \right|_{V_o=0} \quad \text{ohms} 
\]

(5.135)

The ratio indicates that the parameter *h*<sub>11</sub> is an impedance parameter with the units of ohms. Because it is the ratio of the input voltage to the input current with the output terminals shorted, it is called the *short-circuit input-impedance parameter*. The subscript 11 of *h*<sub>11</sub> refers to the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

**h**<sub>12</sub> If *I*<sub>i</sub> is set equal to zero by opening the input leads, the following results for *h*<sub>12</sub>:  

\[
 h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i=0} \quad \text{unitless} 
\]

(5.136)

The parameter *h*<sub>12</sub>, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units because it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter*. The subscript 12 of *h*<sub>12</sub> indicates that the parameter is a transfer quantity determined by a ratio of input (1) to output (2) measurements. The first integer of the subscript defines the measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term reverse is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

**h**<sub>21</sub> If in Eq. (5.134) *V*<sub>o</sub> is set equal to zero by again shorting the output terminals, the following results for *h*<sub>21</sub>:  

\[
 h_{21} = \left. \frac{I_o}{I_i} \right|_{V_o=0} \quad \text{unitless} 
\]

(5.137)

Note that we now have the ratio of an output quantity to an input quantity. The term forward will now be used rather than reverse as indicated for *h*<sub>12</sub>. The parameter *h*<sub>21</sub> is the ratio of the output current to the input current with the output terminals shorted. This parameter, like *h*<sub>12</sub>, has no units because it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter*. The subscript 21 again indicates that it is a transfer parameter with the output quantity (2) in the numerator and the input quantity (1) in the denominator.

**h**<sub>22</sub> The last parameter, *h*<sub>22</sub>, can be found by again opening the input leads to set *I*<sub>i</sub> = 0 and solving for *h*<sub>22</sub> in Eq. (5.134):

\[
 h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i=0} \quad \text{siemens} 
\]

(5.138)

Because it is the ratio of the output current to the output voltage, it is the output conductance parameter, and it is measured in siemens (S). It is called the *open-circuit output admittance parameter*. The subscript 22 indicates that it is determined by a ratio of output quantities.
Because each term of Eq. (5.133) has the unit volt, let us apply Kirchhoff's voltage law “in reverse” to find a circuit that “fits” the equation. Performing this operation results in the circuit of Fig. 5.94. Because the parameter $h_{11}$ has the unit ohm, it is represented by a resistor in Fig. 5.94. The quantity $h_{12}$ is dimensionless and therefore simply appears as a multiplying factor of the “feedback” term in the input circuit.

Because each term of Eq. (5.134) has the units of current, let us now apply Kirchhoff's current law “in reverse” to obtain the circuit of Fig. 5.95. Because $h_{22}$ has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ($1/h_{22}$).

The complete “ac” equivalent circuit for the basic three-terminal linear device is indicated in Fig. 5.96 with a new set of subscripts for the $h$-parameters. The notation of Fig. 5.96 is of a more practical nature because it relates the $h$-parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

- $h_{11} \rightarrow$ input resistance $\rightarrow h_i$
- $h_{12} \rightarrow$ reverse transfer voltage ratio $\rightarrow h_r$
- $h_{21} \rightarrow$ forward transfer current ratio $\rightarrow h_f$
- $h_{22} \rightarrow$ output conductance $\rightarrow h_o$

The circuit of Fig. 5.96 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, they are all three-terminal configurations, so that the resulting equivalent circuit will have the same format as shown in Fig. 5.96. In each case, the bottom of the input and output sections of the network of Fig. 5.96 can be connected as shown in Fig. 5.97 because the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The $h$-parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second
subscript has been added to the \( h \)-parameter notation. For the common-base configuration, the lowercase letter \( b \) was added, whereas for the common-emitter and common-collector configurations, the letters \( e \) and \( c \) were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 5.97. Note that \( I_i = I_b, I_o = I_c \), and, through an application of Kirchhoff's current law, \( I_e = I_b + I_c \). The input voltage is now \( V_{be} \), with the output voltage \( V_{ce} \). For the common-base configuration of Fig. 5.98, \( I_i = I_e, I_o = I_c \) with \( V_{eb} = V_i \) and \( V_{cb} = V_o \). The networks of Figs. 5.97 and 5.98 are applicable for \( pnp \) or \( npn \) transistors.

The input voltage is now \( V_{be} \), with the output voltage \( V_{ce} \). For the common-base configuration of Fig. 5.98, \( I_i = I_e, I_o = I_c \) with \( V_{eb} = V_i \) and \( V_{cb} = V_o \). The networks of Figs. 5.97 and 5.98 are applicable for \( pnp \) or \( npn \) transistors.

The fact that both a Thévenin and a Norton circuit appear in the circuit of Fig. 5.96 was further impetus for calling the resultant circuit a hybrid equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the \( z \)-parameter and \( y \)-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Appendix A the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired small-signal equivalent network for the transistor.

For the common-emitter and common-base configurations, the magnitude of \( h_r \) and \( h_o \) is often such that the results obtained for the important parameters such as \( Z_i, Z_o, A_v \), and \( A_i \) are only slightly affected if \( h_r \) and \( h_o \) are not included in the model.

Because \( h_r \) is normally a relatively small quantity, its removal is approximated by \( h_r \approx 0 \) and \( h_o V_o = 0 \), resulting in a short-circuit equivalent for the feedback element as shown in Fig. 5.99. The resistance determined by \( 1/h_o \) is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 5.99.

The resulting equivalent of Fig. 5.100 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the \( r_e \) model. In fact,
the hybrid equivalent and the $r_e$ models for each configuration are repeated in Fig. 5.101 for comparison. It should be reasonably clear from Fig. 5.101a that

$$h_{ie} = \beta r_e$$  \hspace{1cm} (5.139)

and

$$h_{fe} = \beta_{ac}$$  \hspace{1cm} (5.140)

From Fig. 5.101b,

$$h_{ib} = r_e$$  \hspace{1cm} (5.141)

and

$$h_{fb} = -\alpha \approx -1$$  \hspace{1cm} (5.142)

In particular, note that the minus sign in Eq. (5.142) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the $r_e$ model of Fig. 5.101b.

**FIG. 5.101**

Hybrid versus $r_e$ model: (a) common-emitter configuration; (b) common-base configuration.

---

**EXAMPLE 5.19** Given $I_E = 2.5 \text{ mA}$, $h_{fe} = 140$, $h_{oe} = 20 \mu S$ ($\mu$hmohm), and $h_{ob} = 0.5 \mu S$, determine:

a. The common-emitter hybrid equivalent circuit.
b. The common-base $r_e$ model.

**Solution:**

a. $r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.5 \text{ mA}} = 10.4 \Omega$

$$h_{ie} = \beta r_e = (140)(10.4 \Omega) = 1.456 \text{ k}\Omega$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20 \mu S} = 50 \text{ k}\Omega$$
Note Fig. 5.102.

**FIG. 5.102**
Common-emitter hybrid equivalent circuit for the parameters of Example 5.19.

\[ I_{b} \triangleq 140 I_{b}, \quad r_{e} = 1.456 \text{k}\Omega, \quad \frac{1}{h_{oe}} = 50 \text{k}\Omega \]

\[ r_{o} = 10.4 \Omega, \quad h_{fe}(b_{ac}) = 140, \quad r_{e} = 1.456 \text{k}\Omega \]

**FIG. 5.103**
Common-base \( r_{e} \) model for the parameters of Example 5.19.

\[ \alpha \triangleq 1, \quad r_{o} = \frac{1}{h_{ob}} = \frac{1}{0.5 \mu S} = 2 \text{M}\Omega \]

\[ h_{fe} = \beta r_{e} \text{ that will vary significantly with } I_{C} \text{ and should be determined at operating levels because it can have a real effect on the gain levels of a transistor amplifier.} \]

**5.20 APPROXIMATE HYBRID EQUIVALENT CIRCUIT**

The analysis using the approximate hybrid equivalent circuit of Fig. 5.104 for the common-emitter configuration and of Fig. 5.105 for the common-base configuration is very similar to that just performed using the \( r_{e} \) model. A brief overview of some of the most important configurations will be included in this section to demonstrate the similarities in approach and the resulting equations.
Because the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the $r_e$ model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as $h_{ie}$, $h_{fe}$, $h_{ib}$, and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the $r_e$ model are related by the following equations, as discussed earlier in this chapter:

$$h_{ie} = \beta r_e, \quad h_{fe} = \beta, \quad h_{oe} = 1/r_o, \quad h_{fb} = -\alpha, \quad \text{and} \quad h_{ib} = r_e.$$

### Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 5.106, the small-signal ac equivalent network will appear as shown in Fig. 5.107 using the approximate common-emitter hybrid equivalent model. Compare the similarities in appearance with Fig. 5.22 and the $r_e$ model analysis. The similarities suggest that the analyses will be quite similar, and the results of one can be directly related to the other.

From Fig. 5.107,

$$Z_i = R_B / h_{ie} \quad \text{(5.143)}$$

From Fig. 5.107,

$$Z_o = R_C / 1 / h_{oe} \quad \text{(5.144)}$$

Using $R' = 1 / h_{oe} R_C$, we obtain

$$V_o = -I_o R' = -I_c R'$$

$$= -h_{fe} I_b R'$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

so that

$$A_v = \frac{V_o}{V_i} = -h_{ie} (R_C / 1 / h_{oe}) / h_{ie} \quad \text{(5.145)}$$

Assuming that $R_B \gg h_{ie}$ and $1 / h_{oe} \geq 10R_C$, we find $I_b \approx I_i$ and $I_o = I_c = h_{fe} I_b = h_{fe} I_i$, and so

$$A_i = \frac{I_o}{I_i} \approx h_{fe} \quad \text{(5.146)}$$
EXAMPLE 5.20   For the network of Fig. 5.108, determine:

a. $Z_i$

b. $Z_o$

c. $A_v$

d. $A_i$

Solution:

a. $Z_i = R_B \parallel h_{ie} = 330 \, \Omega \parallel 1.175 \, \Omega$

$d \equiv h_{ie} = 1.171 \, \Omega$

b. $r_o = \frac{1}{h_{oe}} = \frac{1}{20 \, \mu A/V} = 50 \, \Omega$

$Z_o = \frac{1}{h_{oe}} \parallel R_C = 50 \, \Omega \parallel 2.7 \, \Omega = 2.56 \, \Omega \equiv R_C$

c. $A_v = -\frac{h_{fe}(R_C / h_{oe})}{h_{ie}} = \frac{-120(2.7 \, \Omega / 50 \, \Omega)}{1.171 \, \Omega} = -262.34$

d. $A_i \equiv h_{fe} = 120$

Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 5.109, the resulting small-signal ac equivalent network will have the same appearance as Fig. 5.107, with $R_B$ replaced by $R' = R_1 \parallel R_2$. 
\[ Z_i = R_1 \parallel R_2 h_{ie} \]  
(5.147)

\[ Z_o \equiv R_C \]  
(5.148)

\[ A_v = -\frac{h_{fe}(R_C \parallel 1/h_{oe})}{h_{ie}} \]  
(5.149)

\[ A_i = \frac{h_{fe}(R_1 \parallel R_2)}{R_1 \parallel R_2 + h_{ie}} \]  
(5.150)

**Unbypassed Emitter-Bias Configuration**

For the CE unbypassed emitter-bias configuration of Fig. 5.110, the small-signal ac model will be the same as Fig. 5.30, with \( \beta r_e \) replaced by \( h_{ie} \) and \( \beta I_b \) by \( h_{fe}I_b \). The analysis will proceed in the same manner.

\[ Z_b \equiv h_{fe} R_E \]  
(5.151)

and

\[ Z_i = R_B \parallel Z_b \]  
(5.152)

\[ Z_o = R_C \]  
(5.153)

\[ A_v = -\frac{h_{fe} R_C}{Z_b} \equiv -\frac{h_{fe} R_C}{h_{fe} R_E} \]  
(5.154)
**Emitter-Follower Configuration**

For the emitter-follower of Fig. 5.38, the small-signal ac model will match that of Fig. 5.111, with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$. The resulting equations will therefore be quite similar.

**$A_i$**

\[
A_i = -\frac{h_{fe}R_B}{R_B + Z_b} \tag{5.155}
\]

or

\[
A_i = -A_v \frac{Z_o}{R_C} \tag{5.156}
\]

**$Z_i$**

\[
Z_b \equiv h_{fe}R_E \tag{5.157}
\]

\[
Z_i = R_B |Z_b| \tag{5.158}
\]

**$Z_o$**  For $Z_o$, the output network defined by the resulting equations will appear as shown in Fig. 5.112. Review the development of the equations in Section 5.8 and

\[
Z_o = R_E \frac{h_{ie}}{1 + h_{fe}}
\]

or, because $1 + h_{fe} \equiv h_{fe}$,

\[
Z_o \equiv R_E \frac{h_{ie}}{h_{fe}} \tag{5.159}
\]
For the voltage gain, the voltage-divider rule can be applied to Fig. 5.112 as follows:

\[
V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}
\]

but, since \(1 + h_{fe} \approx h_{fe}\),

\[
A_v = \frac{V_o}{V_i} \approx \frac{R_E}{R_E + h_{ie}/h_{fe}}
\]  \(5.160\)

**A_i**

\[
A_i = \frac{h_{fe}R_B}{R_B + Z_b}
\]  \(5.161\)

or

\[
A_i = -A_v \frac{Z_i}{R_E}
\]  \(5.162\)

**Common-Base Configuration**

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 5.113. Substituting the approximate common-base hybrid equivalent model results in the network of Fig. 5.114, which is very similar to Fig. 5.44.

We have the following results from Fig. 5.114.

**Z_i**

\[
Z_i = R_E h_{ib}
\]  \(5.163\)

**Z_o**

\[
Z_o = R_C
\]  \(5.164\)
\[ A_v = \frac{V_o}{I_o} = -(h_{fb}I_e)R_C \]

with

\[ I_e = \frac{V_i}{h_{ib}} \text{ and } V_o = -h_{fb} \frac{V_i}{h_{ib}}R_C \]

so that

\[ A_v = \frac{V_o}{V_i} = -\frac{h_{fb}R_C}{h_{ib}} \]

(5.165)

\[ A_i = \frac{I_o}{I_i} = h_{fb} \equiv -1 \]

(5.166)

**EXAMPLE 5.21** For the network of Fig. 5.115, determine:

a. \( Z_i \)

b. \( Z_o \)

c. \( A_v \)

d. \( A_i \)

![FIG. 5.115 Example 5.21.](image)

**Solution:**

a. \( Z_i = R_E \parallel h_{ib} = 2.2 \, \text{k}\Omega \parallel 14.3 \, \Omega = 14.21 \, \Omega \equiv h_{ib} \)

b. \( r_o = \frac{1}{h_{ob}} = \frac{1}{0.5 \, \mu \text{A/V}} = 2 \, \text{M}\Omega \)

\[ Z_o = \frac{1}{h_{ob}} \parallel R_C \equiv R_C = 3.3 \, \text{k}\Omega \]

c. \[ A_v = -\frac{h_{fb}R_C}{h_{ib}} = -\frac{(-0.99)(3.3 \, \text{k}\Omega)}{14.21} = 229.91 \]

d. \( A_i \equiv h_{fb} = -1 \)

The remaining configurations that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the \( r_o \) or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

### 5.21 COMPLETE HYBRID EQUIVALENT MODEL

The analysis of Section 5.20 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the effect of \( h_r \) and define in more specific terms the effect of \( h_o \). It is important to realize that because the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to